PTO/SB/58 (09-04)
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(Also referred to as FORM PTO-1465)

REQUEST FOR *INTER PARTES* REEXAMINATION TRANSMITTAL FORM

O I P E
OCT 0 2 2006
PATENT & TRADEMARK OFFICE
JAP59

Address to:
Mail Stop *Inter Partes* Reexam
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attorney Docket No.: 38512.3

Date: August 8, 2006

1. [X] This is a request for *inter partes* reexamination pursuant to 37 CFR 1.913 of patent number 6,426,916 issued July 30, 2002. The request is made by a third party requester, identified herein below.

2. [X] a. The name and address of the person requesting reexamination is:
   David L. McCombs, Haynes and Boone, LLP
   901 Main Street, Suite 3100
   Dallas, Texas 75202

   b. The real party in interest (37 CFR 1.915(b)(8)) is: Samsung Electronics Ltd.

3. [X] a. A check in the amount of $ 8800.00 is enclosed to cover the reexamination fee, 37 CFR 1.20(c)(2);

   [ ] b. The Director is hereby authorized to charge the fee as set forth in 37 CFR 1.20(c)(2) to Deposit Account No. ____________ (submit duplicative copy for fee processing); or

   [ ] c. Payment by credit card. Form PTO-2038 is attached.

4. [X] Any refund should be made by [ ] check or [X] credit to Deposit Account No. 08-1394. 37 CFR 1.26(c). If payment is made by credit card, refund must be made to credit card account.

5. [X] A copy of the patent to be reexamined having a double column format on one side of a separate paper is enclosed. 37 CFR 1.915(b)(5)

6. [ ] CD-ROM or CD-R in duplicate, Computer Program (Appendix) or large table
   [ ] Landscape Table on CD

7. [ ] Nucleotide and/or Amino Acid Sequence Submission
   If applicable, items a. – c. are required.

   a. [ ] Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i [ ] CD-ROM (2 copies) or CD-R (2 copies); or
      ii [ ] paper
   c. [ ] Statements verifying identity of above copies

8. [ ] A copy of any disclaimer, certificate of correction or reexamination certificate issued in the patent is included.

9. [X] Reexamination of claim(s) 1-41 is requested.

10. [X] A copy of every patent or printed publication relied upon is submitted herewith including a listing thereof on Form PTO/SB/08, PTO-1449, or equivalent.

11. [X] An English language translation of all necessary and pertinent non-English language patents and/or printed publications is included.

This collection of information is required by 37 CFR 1.915. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Mail Stop *Inter Partes* Reexam, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

12. [X] The attached detailed request includes at least the following items:

a. A statement identifying each substantial new question of patentability based on prior patents and printed publications. 37 CFR 1.915(b)(3)
b. An identification of every claim for which reexamination is requested, and a detailed explanation of the pertinency and manner of applying the cited art to every claim for which reexamination is requested. 37 CFR 1.915(b)(1) and (3)

13. [X] It is certified that the estoppel provisions of 37 CFR 1.907 do not prohibit this reexamination. 37 CFR 1.915(b)(7)

14. [X] a. It is certified that a copy of this request has been served in its entirety on the patent owner as provided in 37 CFR 1.33(c).
The name and address of the party served and the date of service are:
Jose Moniz
Rambus Inc.
4440 El Camino Real, Los Altos, CA 94022

Date of Service: August 8, 2006; or

[ ] b. A duplicate copy is enclosed since service on patent owner was not possible.

15. Correspondence Address: Direct all communications about the application to:

[X] The address associated with Customer Number: 00027683

OR

[ ] Firm or Individual Name		
Address		
City	State	Zip
Country		
Telephone	Fax	

16. [X] The patent is currently the subject of the following concurrent proceeding(s):
[ ] a. Copending reissue Application No. ______.
[ ] b. Copending reexamination Control No. ______.
[ ] c. Copending Interference No. ______.
[X] d. Copending litigation styled:
Rambus Inc. v. Samsung Electronics Ltd., et al.
No. C 05 02298 RMW (N.D. Cal. 2006)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

[signature] — August 8, 2006
Authorized Signature For Third Party Requester — Date

David L. McCombs — 32,271
Typed/Printed Name — Registration Number, if applicable

R95781.1

In place of PTO-1449 Form	U. S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*		Application Number	Ex Parte Reexamination of 6,426,916
		Filing Date	Herewith
		Applicant(s)	...
		Art Unit	*To be Determined*
		Examiner Name	*To be Determined*
SHEET 1 (Exhibits)	OF 3 (Exhibits)	Attorney Docket Number	38512.3

U. S. PATENT DOCUMENTS

Examiner's Initials	Exhibit	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
	A	6,426,916	07-30-2002	Farmwald, et al.
	B	5,590,086	12-31-1996	Park, et al.
	F	4,480,307	10-30-1984	Budde, et al.
	G	4,315,308	02-09-1982	Jackson
	J	4,933,910	06-12-1990	Olson, et al.
	K	5,361,277	03-30-1989	11-01-1994

FOREIGN PATENT DOCUMENTS

Examiner's Initials	Exhibit	Foreign Patent Document	Publication Date MM-DD-YYYY	Patentee or Applicant of Cited Document	Translation Y/N
	I	JP S56-047996	04-30-1981	Yoshida	Yes
	L	GB 2197553	05-18-1988	Lofgren, et al.	

NON-PATENT LITERATURE DOCUMENTS

Examiner's Initials	Exhibit	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city/country where published
	C	Joint Electron Device Engineering Council (JEDEC) Standard No. 21-C, Revision 9 published in 1999 ("JEDEC Standard")
	D, Tab 1	Hyundai, HY5DV651622, Rev. 0.9, published January 2000 ("Hynix -1")
	D, Tab 2	Hyundai, SDRAM Timing Diagram, Rev. 1.2, published December 1999 ("Hynix -2")
	D, Tab 3	Hyundai, DDR SDRAM DEVICE OPERATION, Rev. 0.2, published December 1998 ("Hynix -3")
	E, Tab 1	Intel Corporation, IAPX 432 Interconnect Architecture Reference Manual, published in 1982 ("the iAPX Manual")
	E, Tab 2	Intel Corporation, Electrical Specifications for iAPX 43204 Bus-Interface Unit (BIU) and iAPX 43205 memory control unit (MCU), published March 1983 ("the iAPX Specification")
	H	Rau et al., The Cydra 5 Departmental Supercomputer Design Philosophies, Decisions, and Tradeoffs, published in January 1989 ("Rau")

Examiner Signature		Date Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.

Customer No. 000027683

In place of PTO-1449 Form	U. S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*		Application Number	Ex Parte Reexamination of 5,794,060
		Filing Date	Herewith
		Applicant(s)	...
		Art Unit	*To be Determined*
		Examiner Name	*To be Determined*
SHEET 2 (Exhibits) OF 3 (Exhibits)		Attorney Docket Number	33142.9

NON-PATENT LITERATURE DOCUMENTS

Examiner's Initials	Exhibit	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city/country where published
	M	Johnson et al., A Variable Delay Line PLL for CPU – Coprocessor Synchronization, IEEE Journal of Solid-State Circuits, vol. 23, no. 5, published October 1988 ("Johnson")
	N	Intel Corporation, Memory Components Handbook, Chapter 1 and Chapter 3, Application Note AP-132, published in 1982 and 1985 ("the iRAM reference")
	O	Claim chart for claims 1-5, 10, 12-16, 18-20, 23, 25-32, 35, 37, and 39-41 based on Park, with additional reference to the JEDEC Standard
	P	Claim chart for claims 1-5, 9-10, 12-16, 18-20, 23, 25-27, 30-32, 35, 37, and 40-41 based on the JEDEC Standard
	Q	Claim chart for claims 1-41 of the '916 patent based on the iAPX Manual, with additional reference to Rau, Yoshida, Olson, Johnson, Lofgren, and Grover
	R	Claim chart for claims 1-41 of the '916 patent based on Budde, with additional reference to Rau, Yoshida, Olson, Johnson, Lofgren, and Grover
	S	Patent Family Tree Chart
	T	File History of the '916 patent
	U	File History of U.S. Patent No. 6,452,863 ("the '863 parent patent") (Tab 1 identifies the original disclosure of the '863 parent patent, and Tab 2 identifies the remaining portions of the file history)
	V	*Rambus Inc. v. Samsung Electronics Ltd., et al.* No. C 05 02298 RMW (N.D. Cal. 2006), Preliminary Infringement Contentions
	W	*Samsung Electronics Co., Ltd., v. Rambus Inc.* No. 3:05cv406 (E.D. Va. 2006), Memorandum Opinion filed July 18, 2006
	X	*Hynix Semiconductor, Inc. et al. v. Rambus Inc.*, No. CV 00-20905 RMW (N.D. Cal. 2005), Joint Claim Construction and Prehearing Statement Pursuant to Patent Local Rule 4-3
	Y	*Hynix Semiconductor, Inc. et al. v. Rambus Inc.*, No. CV 00-20905 RMW (N.D. Cal. 2005), Claim Construction Order filed Nov. 15, 2004
	Z	Selected Excerpts from the Trial Transcript from *Hynix Semiconductor, Inc. et al. v. Rambus Inc.*, No. CV 00-20905 RMW (N.D. Cal. 2005).
	AA	*Rambus Inc. v. Infineon Technologies et al.*, No. 3:00cv524 (E.D. Vir. 2001), Memorandum Opinion
	AB	*Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081 (Fed. Cir. 2003)

Examiner Signature		Date Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.

Customer No. 000027683

In place of PTO-1449 Form	U. S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	Ex Parte Reexamination of 5,794,060
				Filing Date	Herewith
				Applicant(s)	...
				Art Unit	*To be Determined*
				Examiner Name	*To be Determined*
SHEET	3 (Exhibits)	OF	3 (Exhibits)	Attorney Docket Number	33142.9

NON-PATENT LITERATURE DOCUMENTS

Examiner's Initials	Exhibit	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city/country where published
	AC	Waters, Hynix Told To Pay Damages To Rambus, Financial Times, April 24 2006
	AD	Poletti, Rambus wins victory from Supreme Court - Win Could Lead To Success For Rambus' Other Lawsuits Seeking Royalties, San Jose Mercury News, Oct. 07, 2003
	AE	Kanellos, Future of memory market hangs on Rambus trials - It's the trial of the century, at least as far as the memory industry is concerned, CNET News.com, Feb. 12, 2001, http://news.com.com/Future+of+memory+market+hangs+on +Rambus+trials/2100-1001_3-252404.html
	AF	Appeal Board Decision dated Feb. 12, 2004, Summary of Facts and Submissions for the oppositions filed against European Patent No. 0 525 068
	AG	Summary of Facts and Submissions for the oppositions filed against European Patent No. 1 004 956
	AH, Tab 1	In the Matter of Rambus, Inc., FTC Docket No. 9302, Opinion of the Commission
	AH, Tab 2	In the Matter of Rambus, Inc., FTC Docket No. 9302, Concurring Opinion of Commissioner Jon Leibowitz
	AH, Tab 3	In the Matter of Rambus, Inc., FTC Opinion Docket No. 9302, Order Reversing and Vacating Initial Decision ...
	AI, Tab 1	Rambus' Final infringement Contentions in the Hynix Litigation
	AI, Tab 2	Exhibit A (accused products) to Rambus' Final infringement Contentions
	AI, Tab 3	Exhibit P ('916 infringement chart) to Rambus' Final infringement Contentions
	AI, Tab 4	Exhibit R (Exemplary data sheet) to Rambus' Final infringement Contentions
	AJ	CD-ROM including present Request for *Inter Partes* Reexamination and Exhibits

Examiner Signature		Date Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Request for *Inter Partes* Reexamination	§	
	§	
U.S. Patent No. 6,426,916	§	REQUEST FOR *INTER PARTES* REEXAMINATION
	§	
Issued: July 30, 2002	§	
	§	
For: MEMORY DEVICE HAVING A VARIABLE DATA OUTPUT LENGTH AND A PROGRAMMABLE REGISTER	§	Attorney Docket No: 38512.3
	§	
	§	Customer No.: 27683
	§	
Requester: Samsung Electronics Ltd.	§	

REQUEST FOR *INTER PARTES* REEXAMINATION UNDER 35 U.S.C. §§ 311-318

Mail Stop *Inter Partes* Reexam
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Dear Sir:

Pursuant to the provisions of 35 U.S.C. §§ 311-318 (2002), the undersigned, on behalf of Samsung Electronics, Inc., the real party in interest, hereby requests an *inter partes* reexamination of all of the claims of United States Patent No. 6,426,916 ("the '916 patent," Exhibit A) that issued on July 30, 2002 to Michael Farmwald *et al.* resulting from a patent application filed on February 27, 2001. In accordance with 37 C.F.R.§ 1.985, notification is hereby provided that the '916 patent is the subject of pending litigation, namely *Rambus Inc. v. Samsung Electronics Ltd., et al.* No. C 05 02298 RMW (N.D. Cal. 2006) (hereinafter "the Samsung Litigation"), and is the subject of former and current litigations, including *Hynix Semiconductor, Inc. et al. v. Rambus Inc.*, No. CV 00-20905 RMW (N.D. Cal. 2000) (hereinafter "the Hynix Litigation"), *Rambus Inc. v. Infineon Technologies et al.*, No. 3:00cv524 (E.D. Vir. 2001) (hereinafter "the Infineon Litigation"), *Micron Technology v. Rambus Inc.*, No. CV 00-792 KAJ (Del. 2000), and *Rambus Inc. v. Micron Technology,* No. CV 00-00244 RMW (N.D. Cal. 2000). In accordance with 37 C.F.R. § 1.915(b)(7), Samsung Electronics Ltd. hereby certifies that the estoppel provisions of 37 C.F.R. § 1.907 do not prohibit this request for *inter partes* reexamination.

The substantial new questions of patentability set forth in this request are precipitated by prior art references that were not cited during the prosecution of the '916 patent, especially when the claims of the '916 patent are construed in the manner proffered by Rambus[1] in its claim constructions and preliminary infringement contentions for the above-referenced litigations, portions of which are included in the attached Exhibits V-AB, and/or in a manner consistent with the claim construction positions proffered by the patentee in the litigations.

For purposes of this request, the Requester will construe all claim language from the claims asserted by the patentee in the manner proffered by Rambus in litigation. Such statements by the patentee may be used by the U.S. Patent and Trademark Office (the "Patent Office") to interpret claim language at issue.[2] By construing the claim language in the manner proffered by Rambus, and/or as otherwise set forth explicitly or implicitly herein, Requester is not admitting and/or acquiescing as to the correctness and/or reasonableness of Rambus' proffered claim construction in the litigation and/or as otherwise set forth herein.

Additionally, with respect to the claims of the '916 patent that have not been asserted by Rambus in litigation, the interpretation and/or construction of such claims presented either implicitly or explicitly herein should not be viewed as constituting, in whole or in part, the Requester's own interpretation and/or construction of such unasserted claims, but instead, should be viewed as constituting an interpretation and/or construction of such unasserted claims that is consistent with Rambus' claim construction positions in the litigation. In fact, the Requester expressly reserves the right to present its own interpretation of such unasserted claims at a later time, which interpretation may differ, in whole or in part, from that presented herein.

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1 Rambus Inc. is listed as the assignee on the front page of the '916 patent, and has asserted that they own the '916 patent in the above-referenced litigations. Rambus Inc. will hereinafter be referred to as "Rambus," "applicant," or "patentee."

2 *See* 37 C.F.R. § 1.104: "In rejecting claims the examiner may rely upon admissions by the applicant, or the patent owner in a reexamination proceeding, as to any matter affecting patentability[.]"

FORWARD

Samsung requests reexamination of the '916 patent in light of the broad interpretations applied by the Court of Appeals for the Federal Circuit to relevant claim terms in the Infineon Litigation and the United States District Court, Northern District of California (Whyte, J.) in the Hynix Litigation.[3] With these rulings as ammunition, Rambus alleges its "patents will be more broadly construed"[4] and claims that the '916 patent reads on virtually all dynamic random access memories (DRAMs) made, used or sold in the United States today, including synchronous DRAMs (SDRAMs) and double data rate SDRAMs (DDR, DDR2). Based on this broad interpretation of the '916 patent (and other patents with the same specification), Rambus received a jury verdict of over $300 million against Hynix for its SDRAM and DDR products (Rambus accused DDR2 and other products in a later lawsuit) in April 2006.[5] The '916 patent and approximately 28 other patents are now being asserted by Rambus against the memory industry, where Rambus is seeking billions of dollars in recoveries and injunctive relief, such as would dwarf the potential impact of *NTP v. Research In Motion (RIM)* case on the U.S. computer industry specifically, and this country's economy as a whole.[6]

The '916 patent is a member of a large patent family owned by Rambus, initiated over 16 years ago by the filing of U.S. Ser. No. 510,898 ("the original '898 application") on April 18, 1990. The extended patent family includes over 30 issued patents and many pending and abandoned applications. The '916 patent is not valid under 35 U.S.C. §§ 102 or 103 when prior art patents and publications are considered in light of the 2001 filing date of the application that resulted in the issuance of that patent. The '916 patent is not entitled to a priority date any earlier than the actual filing date of its application because the Federal Circuit in the Infineon Litigation

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3 *Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1094 (Fed. Cir. 2003), Exhibit AB and *Hynix Semiconductor, Inc. et al. v. Rambus Inc.*, No. CV 00-20905 RMW (N.D. Cal. 2005), Claim Construction Order, Exhibit Y.

4 Poletti, Rambus wins victory from Supreme Court - Win Could Lead To Success For Rambus' Other Lawsuits Seeking Royalties, San Jose Mercury News, Oct. 07, 2003, Exhibit AD.

5 Waters, Hynix Told To Pay Damages To Rambus, Financial Times, April 24 2006, Exhibit AC. To avoid a new trial on the issue of damages, Rambus agreed to accept a remittitur of the jury award to approximately $133 Million.

6 Kanellos, Future of memory market hangs on Rambus trials - It's the trial of the century, at least as far as the memory industry is concerned, CNET News.com, Feb. 12, 2001, Exhibit AE.

and Judge Whyte in the Hynix Litigation adopted a construction of the term "bus" and other key terms used in the claims, in a manner which cannot be supported by the specification of the original '898 application, as explained fully in the present request. Notwithstanding, even if priority to the original '898 application were to apply, the claims are still invalid under §§ 102 and 103 in light of arguments relating to prior patents and publications dating to the early 1980s not previously presented to the Patent Office.

It is not surprising that Rambus is unable to support the claims of the '916 patent with a priority date earlier than the date of its immediate application because, as recently found in a July 19, 2006 opinion by Judge Robert Payne of the U.S. District Court for the Eastern District of Virginia, Rambus' prosecution attorney of record for the '916 patent, Neil Steinberg, deliberately re-wrote the claims of this patent to cover products being manufactured in the late 1990s, years after the original '898 application was drafted and filed. As stated by the Court:

> Also, in late 1991, Rambus joined JEDEC and, as reflected in the company's 1992 business plan, learned that JEDEC was formulating a standard applicable to SDRAMs. The process of developing the standard was a slow one. As Rambus attended the meetings, its representatives, Crisp and Garrett, obtained information that was used to improve existing applications or to file new ones in a deliberate effort to cover the evolving SDRAM standard.
>
> Further, Steinberg ascertained that some of the pending applications might not be effective in covering SDRAM products to be made in compliance with JEDEC standard. Therefore, he took over the patent prosecution of a number of patents in 1998 with a view to strengthening the Rambus portfolio as to SDRAM and DDR-DRAM products.
>
> . . .
>
> The next slide, Strategy Update, 10/98-2, specifies that Rambus should give top priority to strengthening its portfolio by filing continuation cases based on the '898 filing in 1990, the object of which was to cover SDRAM, DDR, SLDRAM, and any and all forms of synchronous memory (static and dynamic). [7]

Judge Payne also found that both Mr. Steinberg and Mr. Karp expressly lied or were "untruthful" in their testimony to the Court:

> Karp's statement in DTX 3691 is but one reason why the Court considers incredible his testimony in both the Infineon and Hynix unclean hands trials that, in 1998 and 1999, Karp and Rambus regarded litigation as unlikely because the goal was to reach settlement. This document, like other contemporaneous business records, substantially

[7] Memorandum Opinion at pgs. 55-57, Exhibit W.

> disproves that and kindred assertions.
>
> Having found that Steinberg has testified falsely on important matters, the Court will not credit his testimony on that point.[8]

On July 31, 2006 the Federal Trade Commission further recognized the nature and scope of Rambus' anticompetitive conduct involving the patent family.[9] As pointed out in the Opinion of the Commission and Concurring Opinion, Rambus secretly used the U.S. patent system to allegedly cover what was intended to be an open DRAM standard:

> Through a course of deceptive conduct, Rambus exploited its participation in JEDEC to obtain patents that would cover technologies incorporated into now –ubiquitous JEDEC memory standards, without revealing its patent position to other JEDEC members. As a result, Rambus was able to distort the standard-setting process and engage in anticompetitive "hold up" of the computer memory industry.[10]
>
> . . .
>
> Here, Rambus used information gained through participation in cooperative JEDEC processes by tailoring its patent claims to facilitate hold-up, while deceiving other JEDEC members regarding its patent position..[11]
>
> . . .
>
> Based on this wolf-in-sheep's-clothing pose, Rambus was in a position to, and did, amend its own patent claims in order to secretly convert what was intended to be an openly available industry-standard into a private source of revenues."[12]
>
> . . .
>
> Rambus continued to use the knowledge gained at JEDEC to amend its patents in this manner. As noted in a December 1992 Rambus planning document, Rambus sought to "get a copy of the SDRAM spec and check it out for features we need to cover as well as features which violate our patents." Crisp's September 1995 statement to Rambus management further sums up Rambus's strategy. He urged Rambus:
>
>> "should redouble our efforts to get the necessary amendments completed, the new claims added and make sure this ship is watertight before we get too far out to sea."[13]

The Commission also noted the tremendous impact Rambus' secretive behaviors could have on the industry: "[t]he total cost of payments for Rambus's undisclosed patents could amount to

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8 Memorandum Opinion at pgs. 60 and 89, Exhibit W. See also, pg. 54, footnote 20.

9 *See, In the Matter of Rambus Incorporated*, Docket No. 9302, Opinion of the Commission (July 31, 2006); Concurring Opinion of Commissioner Jon Liebowitz in the Matter of Rambus, Inc. (July 31, 2006); and Order Reversing and Vacating Initial Decision and Accompanying Order, Scheduling Supplemental Briefing on the Issues of Remedy, and Denying Complaint Counsel's Motion for Sanctions (July 31, 2006) (Exhibit AH, Tabs 1, 2, and 3).

10 Opinion of the Commission at pg. 3, Exhibit AH, Tab 1.

11 Id. at pg. 67.

12 Concurring Opinion at pg. 19, Exhibit AH, Tab 2.

13 Id. at pg. 19, citing CX 837 at 2.

several billion dollar, with some individual DRAM manufacturers each paying hundreds of millions of dollars. Numbers of this magnitude are not easily overlooked."[14] (citations omitted). Especially in light of the fact that royalty rates Rambus attempts to impose on the industry are "*not* reasonable."[15]

Rambus' prosecution and litigation tactics regarding this patent family have "made it one of the most prominent targets of critics who claim that abuse of the US patent system exposes tech companies to unfair claims."[16] It is with this request for reexamination of the '916 patent, as set forth below, that the Requester hopes to bring a halt to Rambus' abuse of the US patent system.

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[14] Opinion of the Commission at pgs. 75-76.

[15] Id. at pg. 115.

[16] Waters, Hynix Told To Pay Damages To Rambus, Financial Times, April 24 2006, quoting Stanford University law professor Mark Lemley, Exhibit AC.

I. Citation Of Claims For Which Reexamination Is Requested And Citation Of Patents And Printed Publications Presented To Provide A Substantial New Question Of Patentability

In accordance with 37 C.F.R. §§ 1.915(b)(1) and (b)(2), reexamination of claims 1-41 (all of the issued claims) of the '916 patent is requested in view of the following references:[17]

Exhibit B	Park et al., U.S. Patent No. 5,590,086 issued December 31, 1996 ("Park")
Exhibit C	Joint Electron Device Engineering Council (JEDEC) Standard No. 21-C, Revision 9 published in 1999 ("the JEDEC Standard")
Exhibit D, Tab 1	Hyundai, HY5DV651622, Rev. 0.9, published January 2000 ("Hynix -1")[18]
Exhibit D, Tab 2	Hyundai, SDRAM Timing Diagram, Rev. 1.2, published December 1999 ("Hynix -2")
Exhibit D, Tab 3	Hyundai, DDR SDRAM DEVICE OPERATION, Rev. 0.2, published December 1998 ("Hynix -3")
Exhibit E, Tab 1	Intel Corporation, iAPX 432 Interconnect Architecture Reference Manual, published in 1982 ("the iAPX Manual")
Exhibit E, Tab 2	Intel Corporation, Electrical Specifications for iAPX 43204 Bus-Interface Unit (BIU) and iAPX 43205 memory control unit (MCU), published March 1983 ("the iAPX Specification")
Exhibit F	Budde et al., U.S. Patent No. 4,480,307 issued October 30, 1984 ("Budde")
Exhibit G	Jackson, U.S. Patent No. 4,315,308 issued February 9, 1982 ("the '308 patent")
Exhibit H	Rau et al., The Cydra 5 Departmental Supercomputer Design Philosophies, Decisions, and Tradeoffs, published in January 1989 ("Rau")
Exhibit I	Yoshida, Japanese Patent JP S56-047996 published April 30, 1981, English translation provided ("Yoshida")
Exhibit J	Olson et al., U.S. Patent No. 4,933,910 issued June 12, 1990 ("Olson")
Exhibit K	Grover, U.S. Patent No. 5,361,277 filed March 30, 1989, issued November 1, 1994 ("Grover")

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[17] References C-G and K-N were presented as prior art references for purposes of invalidity in the Hynix Litigation. Although the jury found that Hynix did not meet its burden of proof regarding its invalidity contentions, the burden of proof is not the same for a reexamination. In addition, the arguments presented in this request for reexamination are not necessarily the same as those presented by Hynix at trial. Also, references C, G, and K are listed as cited references to the '916 patent. The fact that a reference was previously cited does not preclude the existence of a substantial new question of patentability "where the art is being presented/viewed in a new light, or in a different way, as compared with its use in earlier concluded examination(s), in view of a material new argument or interpretation presented in the request." See MPEP § 2258.01.

[18] Hyundai Electronics became Hynix Semiconductor in 2001.

Exhibit L	Lofgren et al., UK published patent app. no. GB2197553, published May 18, 1988 ("Lofgren")
Exhibit M	Johnson et al., A Variable Delay Line PLL for CPU – Coprocessor Synchronization, IEEE Journal of Solid-State Circuits, vol. 23, no. 5, published October 1988 ("Johnson")
Exhibit N	Intel Corporation, Memory Components Handbook, Chapter 1 and Chapter 3, Application Note AP-132, published in 1982 and 1985 ("the iRAM reference")

A complete listing of all the Exhibits, including claim charts, file histories, and other documents, is provided at the end of the present request.

II. Statement Under 37 C.F.R. § 1.915(b)(3) Of Each Substantial New Question Of Patentability Based Upon Previously Uncited Prior Art

The claims of the '916 patent are fully anticipated under 35 U.S.C. §102 by, and/or are unpatentable under 35 U.S.C. §103 in view of several different prior art references which were not previously considered during the examination of the '916 patent. Claims 1-41 of the '916 patent are set forth in detail on the attached claim charts (Exhibits O-R) that compare the limitations of the claims to the pertinent prior art references. As the claim charts demonstrate, claims 1-41 of the '916 patent are invalid under 35 U.S.C. § 102 and/or 35 U.S.C. § 103 in view of the previously unconsidered prior art references under any reasonable interpretation of the claims, and especially when the claims are interpreted in the manner proffered by the patentee, Rambus, in the above-referenced litigations.

The following analysis is separated into two sections. The first section is directed to printed publications that are prior to February 27, 2001, the filing date of the '916 patent. The first section also includes an analysis of why the claims of the '916 patent are not entitled to a priority date earlier than February 27, 2001. Determining the priority date for claims of a patent in an extended patent family is appropriate for an *inter partes* proceeding. See MPEP § 2617. The second section is directed to printed publications that are prior to April 18, 1990, the filing date of the original '898 patent application and the earliest possible priority date of the '916 patent.

SECTION ONE:
Rejection Of Claims 1-5, 9-20, 23, 25-41 In View Of Publications Prior To February 27, 2001, The Filing Date Of The '916 Patent

The MPEP expressly states that determining the correct priority date of a claim is appropriate for an *inter partes* proceeding. Specifically, MPEP § 2617 permits the requester to "point out that claims in the patent for which reexamination is requested are not supported by an earlier foreign or United States patent application whose filing date is claimed." Here, the '916 patent belongs to a 10+ year patent family comprising multiple patents and patent applications dating back to the original '898 application filed on April 18, 1990. Although all of the patents and patent applications are identified as either continuations or divisionals, claims 1-5, 9-20, 23, 25-41 of the '916 patent purport to claim subject matter that is not supported by the original '898 application. In fact, these claims of the '916 patent are not even entitled to the priority date of its immediate parent, U.S. Patent No. 6,452,863 ("the '863 parent patent").

The following discussion describes the legal requirements for priority, identifies the original disclosure of the '863 parent patent, and provides multiple reasons why claims 1-5, 9-20, 23, and 25-41 of the '916 patent are not supported by the original disclosure of the '863 parent patent. Following the priority discussion, this section of the present request further establishes the unpatentability of these claims based upon publications that are prior art to February 27, 2001 - the filing date of the '916 patent.

A. The Claims Of The '916 Patent Are Not Entitled To A Priority Date Earlier Than February 27, 2001 – The Filing Date Of The '916 Patent

As discussed above in the Forward, the '916 patent was filed by Rambus in an effort to expand the scope of the disclosure of the original '898 application to unsupported subject matter – purporting to cover conventional SDRAMs. This becomes very clear when the claims are considered in light of the previous claim construction being asserted by Rambus and adopted by the Federal Circuit. Specifically, the Federal Circuit ruled (pre-*Phillips*) that the claim term "bus" should be interpreted under the ordinary meaning of the term, and to not specifically

require a multiplexed bus.[19] As discussed below, claims 1-5, 9-20, 23, and 25-41 of the '916 patent are not supported by the original disclosure of the '863 parent patent, and therefore are not entitled to a claim of priority beyond its own filing date.

1. The Legal Requirements for Claiming Priority

35 U.S.C. § 120 states that

> An application for patent for an invention disclosed in the manner provided by the first paragraph of section 112 of this title in an application previously filed in the United States, or as provided by section 363 of this title, which is filed by an inventor or inventors named in the previously filed application shall have the same effect, as to such invention, as though filed on the date of the prior application[.]

The first paragraph of 35 U.S.C. § 112 states that

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The MPEP further states that "to be entitled to an earlier priority date or filing date under 35 U.S.C. §§ 119, 120, or 365(c), each claim limitation must be expressly, implicitly, or inherently supported in the originally filed disclosure." MPEP § 2163 II.A.3(b). Thus in determining the priority date for the claims of the '916 patent, the original disclosure of the parent patent to which priority is being sought must be identified, and the claims of the '916 patent can then be compared to the original disclosure. As will be shown in detail below, the original disclosure of the '863 parent patent[20] does not support claims 1-5, 9-10, 12-20, 23, 25-32, 34-35, 37, and 39-41 of the '916 patent under § 112 of the patent laws, and these claims of

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[19] *Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1094 (Fed. Cir. 2003), Exhibit AB. Note that this Federal Circuit opinion was issued prior to the case *Phillips v. AWH*, 415 F.3d 1303, 1312 (Fed. Cir. 2005). Under *Phillips*, claims are to be interpreted based on the context of the intrinsic evidence (patent claims, specification, and file history) rather than under the methodology of *Texas Digital Systems, Inc. v. Telegenix, Inc.*, 308 F.3d 1195 (Fed. Cir. 2002), which placed too much reliance on extrinsic sources such as dictionaries. The Requestor believes that when the claims are interpreted in light of the intrinsic evidence, as set forth in this request for reexamination, the claims require a multiplexed bus.

[20] The '863 parent patent was the only patent listed in the priority claim of the '916 patent that was pending at the time the '916 patent was filed. Therefore, if the original disclosure of the '863 parent patent does not support a claim of priority, then the rule of "continuity of disclosure" prevents analysis of other listed patents for such priority. See *Lemelson v. TRW, Inc.*, 760 F.2d 1254, 1266-67 (Fed. Cir. 1985).

the '916 patent are therefore not entitled to claim priority to the '863 parent patent under 35 U.S.C. § 120.

2. The Original Disclosure of U.S. Patent No. 6,452,863

The '863 parent patent is the immediate parent to the '916 patent. The application for the '863 parent patent was filed with a photocopy of the '898 original patent application dating back to April 18, 1990 (U.S. Ser. No. 510,898), along with a photocopy of the original declaration for the '898 original application and a preliminary amendment that cancelled the 150 claims of the '898 original application and added an entire new set of 41 claims. See Exhibit U, Tab 1, pgs. 8-132, 159-168. The original '863 declaration makes no reference to the preliminary amendment, nor does the original 1990 declaration for the '898 application. Id. at pgs. 133-134.

A preliminary amendment that is present on the filing date of the application "does not enjoy the status as part of the original disclosure in an application filed under 37 CFR § 1.53(b) accompanied by a signed oath or declaration *unless it is referred to in the oath or declaration filed therewith*."[21] Because the oaths filed with the '863 parent patent and original 1990 application did not reference the preliminary amendment, the preliminary amendment is not part of the original disclosure of the '863 parent patent and cannot be relied on for a claim of priority to the '863 parent patent. Therefore, the original disclosure of the '863 parent patent consists entirely of the photocopy of the '898 original application and does not include the subject matter contained within the preliminary amendment. Any additional subject matter in the preliminary amendment is not entitled to claim the priority date of the '863 parent patent.[22]

The following analysis will compare the claims of the '916 patent to the original disclosure of the '863 parent patent, i.e., the photocopy of the '898 original application to show that claims 1-5, 9-20, 23, and 25-41 are not supported by the '898 original application.

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21 MPEP §608.04(b), 7th Ed., Revised February 2000, emphasis added.

22 If the claims of the preliminary amendment in the '863 parent patent are considered part of its original disclosure, there are additional reasons that the claims of the '916 patent are not entitled to a priority date of the '898 original patent application.

3. Claims 1-41 Of The '916 Patent Are Not Supported By The Original Disclosure Of The '863 Parent Patent

As will be discussed in greater detail below, there are several, independent reasons why one or more claims of the '916 patent are not supported by the original disclosure of the '863 parent patent under 35 U.S.C. § 112, and are thus not entitled to a priority date earlier than February 27, 2001, the filing date of the '916 patent. The Federal Circuit has ruled that the term "bus", as used in the claims, "does not require a multiplexing bus with respect to a related Rambus patent."[23] The Federal Circuit did not analyze or rule, however, on whether the claims of the patents as so-construed are supported by the original disclosure of the original '898 application.

<u>a. The original disclosure of the '863 patent does not provide Written Description support for claims 1-5, 9-10, 12-20, 23, 25-32, 34-35, 37, and 39-41 of the '916 patent because these claims are missing an essential element</u>

According to Rambus, claims 1-5, 9-10, 12-20, 23, 25-32, 34-35, 37, and 39-41 do not require a multiplexed bus. However, as will be discussed in greater detail below, the multiplexed bus is an essential element of the original disclosure of the '863 parent patent. Accordingly, these claims are not entitled to claim priority to the '863 parent patent.

Section 2163.05 (I) of the MPEP describes that "[u]nder certain circumstances, *omission of a limitation* can raise an issue regarding whether the inventor had possession of a broader, more generic invention." (Emphasis added.) This section of the MPEP goes on to state that "[a] claim that omits an element which the applicant describes as an essential or critical feature of the invention originally disclosed does not comply with the written description requirement."[24]

The MPEP further describes several Federal Circuit cases for support of this rule. The MPEP cites *Tronzo v. Biomet*, which states that "claims to generic cup shape were not entitled to filing date of parent application which disclosed 'conical cup' in view of the disclosure of the parent application stating the advantages and importance of the conical shape." The facts of the

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23 *Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1095 (Fed. Cir. 2003), Exhibit AB. Note that this Federal Circuit opinion was issued prior to *Phillips v. AWH*, 415 F.3d 1303, 1312 (Fed. Cir. 2005).

24 Section 2172.01 further states that "[a] claim which omits matter disclosed to be essential to the invention as described in the specification or other statements of record may be rejected under 35 U.S.C. 112, first paragraph, as not enabling."

Tronzo v. Biomet case are in principle identical to the present situation, in which the parent application states the advantages and importance of the multiplexed bus and then the '916 patent attempts to improperly broaden the scope of the claims by omitting the critical feature of the invention. The broader claims attempt to bring into the scope of the '916 patent exactly that which it proffered as being distinguishable over and wrong with the prior art: separate address, control, and data lines. This contradicts every section of the original disclosure, which explicitly describes the multiplexed bus as the essential element of the alleged invention.

The TITLE of the original 1990 application, "Integrated Circuit I/O Using a High Performance Bus Interface", is consistent with the remainder of the specification disclosing a specialized bus and an interface for connecting to the specialized bus. Exhibit U, Tab 1, pg. 8 (pg. 1, lns. 5-6 of the Application).

The FIELD OF THE INVENTION section of the original disclosure of the '863 patent states that the alleged invention is directed to "[a]n integrated circuit bus interface for computer and video systems [is described] which allows high speed transfer of blocks of data, particularly to and from memory devices with reduced power consumption and increased system reliability. A new method of physically implementing the bus architecture is also described." Id. at pg. 8 (pg. 1, lns. 10-15 of the Application).

The BACKGROUND OF THE INVENTION section attempts to differentiate the multiplexed bus by stating that, "[t]o understand the concept of the present invention, it is helpful to review the architecture of conventional memory devices." Id. at pg. 9 (pg. 2, lns. 7-9 of Application). "Each [conventional] memory device typically is connected in parallel to a series of address lines and connected to one of a series of data lines." Id. at pg. 8 (pg. 1, lns. 22-24 of the Application). Thus, the concept of the present invention of the '916 patent is a multiplexed bus, in contrast to separate address and data lines.

The COMPARISON WITH PRIOR ART section distinguishes one prior art reference stating that the prior art's "external interface is conventional, with separate control, address and data connections." Col. 2, lns. 34-35. This distinction is meaningless without a requirement of a multiplexed bus. Another prior art reference was distinguished because "[t]here are separate pins for data and control (RAS, CAS, WE, CS)." Col. 2, lns. 47-48. Again, this distinction is meaningless without a requirement of a multiplexed bus. Additional prior art was distinguished because "[n]one of the buses described in patents or other literature use only bused connections."

Col. 3, lns. 2-4. Clearly, the patentee was directing the Patent Office away from such prior art references because they did not have a multiplexed bus. One would not understand the inventors to be in possession of an alternate way of transmitting information to and from a memory device other than over a multiplexed bus.

The COMPARISON WITH PRIOR ART section also describes seven "objects" of the invention that all directly or indirectly describe the multiplexed bus or how to interface devices using packet-based addressing techniques for the multiplexed bus.[25] The description of the prior art memory systems emphasizes that address, control and data use separate connections and that the prior art did not bus substantially all signals to and from the memory device. Specifically, in describing the prior art, the application notes that "not all of the interfaces between the devices are bused." Id. at pg. 10 (pg. 3, lns. 15-16 of the Application). This section also teaches that signals going to and from the memory device that have separate connections for control, address and data should be avoided.

The SUMMARY OF THE INVENTION section describes the invention as including "a memory subsystem comprising at least two semiconductor devices, including at least one memory device, connected in parallel to a bus, where the bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by said memory devices...". Id. at pg. 14 (pg. 7, lns. 10-15 of the Application). The summary also describes the multiplexed bus when it states that "[i]n the system of this invention, DRAMs and other devices receive address and control information over the bus and transmit or receive requested data over the same bus." Id. at pg. 15 (pg. 8, lns. 9-11 of the Application). The features of the bus are again emphasized in this section and purport to achieve the improvement over the prior art described in the Comparison with Prior Art section. Therefore, the multiplexed bus (carrying substantially all address, data and control information, including device select information) is <u>the essential element</u> of the invention.

The SUMMARY OF THE INVENTION section also teaches that the memories in this multiplexed bus system, unlike conventional memories, must have a single bus interface with no

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[25] Id. at pgs. 14-15 (pg. 6, ln. 8 – pg. 7, ln. 7 of the Application). The memory devices of the '916 patent are provided with a "unique identifier," or "device ID number," that is part of the message packets being sent on the multiplexed bus. The device ID number allows devices to identify packets on the bus, and supports dynamically "mapping out" bad devices. This is described in greater detail in the section of the DETAILED DESCRIPTION titled "Device Address Mapping." Id. at pgs. 24-25 (pg. 16, ln. 9 – pg. 18, ln. 19 of the Application).

other signal pins to connect to the bus. ("Each memory device contains only a single bus interface with no other signal pins." Id. at pg. 15 (pg. 8, lns. 11-13 of the Application)). Accordingly, the summary further teaches that "[n]ew bus interfaces circuits *must be* added[to the DRAMs]." Id. at pgs. 15-16 (pg. 8, ln. 25 – pg. 9, ln. 3 of the Application), emphasis added. "This *requires* changes to the [DRAM internal circuitry.]" Id. at pg. 16 (pg. 9, lns. 3-4 of the Application), emphasis added. In particular, a standard DRAM "is modified to use a wholly bus-based interface rather than the prior art combination of point-to-point and bus based wiring used with conventional versions of these devices." Id. at pg. 14 (pg. 7, lns. 22-25 of the Application).

The first sentence of the DETAILED DESCRIPTION section states that "[t]he present invention is designed to provide a high speed, multiplexed bus for communication between processing devices and memory devices and to provide devices adapted for use in the bus system." Id. at pg. 18 (pg. 11, lns. 16-19 of Application). The description then affirmatively states that "[t]here is *no need* for separate address and data lines because address and data information can be sent over the same lines." Id. at pg. 19 (pg. 12, lns. 5-6 of the Application), emphasis added. This introduction to the detailed description of the invention once again establishes the importance of the features of the multiplexed bus, and explicitly teaches against using a non-multiplexed bus. It also describes the alleged invention as a multiplexed bus and devices especially adapted for using the bus. Since the memory devices must be adapted to use the multiplexed bus, these devices must also comply with the essential features of the multiplexed bus. The detailed description section refers to "the bus" and since only a multiplexed bus is described, the applicant must be referring to the bus described at the beginning of the detailed description section. See, e.g., "The bus uses relatively simple, synchronous...." in the Protocol and Bus Operation section. Id. at pg. 26 (pg. 19, lns. 24-25 of the Application).

A removal of the multiplexed bus would have far reaching consequences not contemplated by the specification. First, the memory devices would not need to be modified as described in the summary section (e.g., no need for single bus interface, multiplexer/demultiplexer). Second, the described packet protocol could not be implemented. Third, the concept of access time information is tied to the existence of the multiplexed bus. Access time, according to the specification, allows "maximum utilization of the bus for transfer of short blocks of data..." Id. at pg. 23 (pg. 16, lns. 2-3 of the Application).

All 150 CLAIMS of the original disclosure of the '863 parent patent are directly or indirectly directed to a multiplexed bus. Specifically, 138 of the claims are directed to a multiplexed bus and/or transferring data using a multiplexed bus, 9 of the claims are directed to a clocking scheme for use with a multiplexed bus, and 3 of the claims are directed to a packaging scheme for use with devices connected to a multiplexed bus.[26]

It is clear from the foregoing that the multiplexed bus is <u>the essential element</u> of the alleged invention. Accordingly, claims 1-5, 9-10, 12-20, 23, 25-32, 34-35, 37, and 39-41 are not supported by the original disclosure of the '863 parent patent under the first paragraph of section 112, and are thus not entitled to priority under 35 U.S.C. § 120.

It should be noted that the European Patent Office's (EPO) Opposition Division determined that a European counterpart to the Rambus family of patents taught a reader that "the features of bus interface [were] essential and indispensable to achieve efficient, high-speed access to blocks of data." Exhibit AG at § 2.5. Therefore the EPO determined that the claims must include a bus that "includes a plurality of bus lines for carrying substantially all address, data and control information needed by said semiconductor memory device." Id. at § 2.6. Additionally, the EPO determined that a system without a multiplexed bus and a system that received a single (versus two) external clock signal were not disclosed in the earlier application.[27] Id. at §§ 2.6, 2.8. Another decision by the EPO Opposition Division relating to a different Rambus European counterpart similarly determined that "the only interpretation of the [bus] feature which is supported by the application as a whole is that the bus is multiplexed" and revoked the EP patent. Exhibit AF at § 4.2. Although the patent laws in Europe differ from those in the United States, the Requester believes that these findings are relevant to the §112 issues raised in this request for reexamination.

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[26] "The bus architecture of this invention makes possible an innovative 3-D packaging technology. By using a narrow, multiplexed (time-shared) bus, the pin count for an arbitrarily large memory device can be kept quite small - on the order of 20 pins." Id. at pg. 49 (pg. 42, lns. 18-22 of the Application).

[27] This earlier application was based on the same application as the original 1990 patent application.

b. The original disclosure of the '863 parent patent does not provide Written Description support for transmitting access time information, block size information, and operation codes in any way other than as parameters of a packet on a multiplexed bus

As stated above, Rambus asserts that claims 1-5, 9-10, 12-20, 23, 25-32, 34-35, 37, and 39-41 do not require a packetized, multiplexed bus. However, these claims further require sending packet parameters including access time information, block size information, and operation codes. Each of the independent claims of the '916 patent includes these limitations, but for the sake of reference, claim 1 describes these limitations as follows:

> [access time information:] receiving a value that is representative of a number of cycles of an external clock signal to transpire after which the memory device responds to a first operation code
>
> [block size information:] receiving block size information, wherein the block size information is representative of an amount of data to be output by the memory device in response to the first operation code
>
> [operation codes:] sampling the first operation code

All of these terms refer to parameters in a packet-based bus system. Furthermore, the patentee relied on this interpretation to distinguish the claims from the prior art, as discussed in the section above with regards to the COMPARISON WITH PRIOR ART section. Therefore, to the extent that access time information, block size information, and operation codes are defined as anything but packet parameters (i.e., part of a packet), as currently being asserted by Rambus, then these claims are not supported by the original disclosure of the '863 parent application. One would not understand the inventors to be in possession of an alternate way of transmitting (and providing) access time information, block size information, and operation codes to a memory device other than as part of a packet over a multiplexed bus.

c. The original disclosure of the '863 patent does not provide Written Description support for claims 1-41 of the '916 patent if they do not require two external clock signals

According to Rambus, claims 1-41 do not require two external clock signals. However, the original disclosure of the '863 parent patent only describes an embodiment that uses two external clock signals. The specification identifies the use of two clock signals (an early and late clock) in order to operate the memory devices. "Clocking a high speed bus accurately without introducing error due to propagation delays can be implemented by having each device monitor two bus clock signals and then derive internally a device clock, the true system clock." Id. at pg.

53 (pg. 46, lns. 20-23 of the Application). Nowhere in the specification does the applicant identify the use of a single external clock. Instead, the specification teaches that two clock signals are necessary, especially in connection with the internal clock generation circuitry. "One important part of the input/output circuitry generates an internal device clock based on early and late bus clocks. Controlling clock skew (the difference in clock timing between devices) is important in a system running with 2 ns cycles, thus the internal device clock is generated so the input sampler and the output driver operate as close in time as possible to midway between the two bus clocks." Id. at pgs. 63-64 (pg. 56, ln. 21 through pg. 57, ln. 2 of the Application). Without the second external clock, however, an essential element is missing from the claims and therefore these claims are not supported by the written description of the '863 parent patent. Thus, these claims cannot claim priority to the '863 parent patent.

d. The original disclosure of the '863 patent does not provide Written Description support for a delayed locked loop as required in claim 40 of the '916 patent

The term "delay locked loop" does not appear in the '863 parent application. The only clocking circuit disclosed appears in Fig. 12. However, this disclosure relates to an internal clock signal synchronized to a time half way between the early and late bus clock signals. This is not what is now commonly known as a delay locked loop, such as the delay locked loop in Lofgren, discussed below. In fact, the applicants claim that the "clocking scheme used in this invention has not been used before...". Col. 9, lns. 9-10. Therefore, one would not understand the inventors to be in possession of a clocking scheme other than the alleged novel clocking scheme disclosed in the specification.

e. The original disclosure of the '863 parent patent does not provide Written Description support for outputting data on the rising and falling edge of an external clock signal as required in claims 3, 18 and 31 of the '916 patent

The '863 parent patent does not disclose outputting data on both the rising and falling edge of an external clock signal. At best, the disclosure indicates that two internal clocks (CLK and /CLK) could operate at half the bus data rate and, if each clock outputs data on one of its

edges (as is done traditionally), the device could output data at the same rate as the bus clock.[28] With the output lines being driven alternately by CLK and /CLK bar as shown in Fig. 10, there would be no need to output on both the rising and falling edges of one clock. Instead, the data would be driven on the rising edge only of each clock, or the falling edge only, but not both. Further, both CLK and /CLK are <u>internal</u> clocks, not an external clock. Therefore, one would not understand the inventors to be in possession of a system that *outputs a portion of data on the rising edge and a portion of the data on the falling edge of an external clock signal.*

In summary, the Examiner may utilize admissions by the patent owner, made in litigation, for patent reexaminations.[29] Accordingly, to the extent the Examiner adopts the claim construction being asserted by Rambus, the Examiner should find that the claims as so construed are not supported by the original disclosure of the '863 parent patent. Therefore, the claims of the '916 patent are not entitled to a priority date beyond its filing date of the '916 patent – February 27, 2001.

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[28] *See* Fig. 10. During the Hynix trial, Rambus' expert identified a passage in the specification (Col. 19, lns. 39-42) as supporting claims with dual edge clocking. Exhibit Z, Hynix trial transcript at pg. 2680, ln. 20 – 2682, ln. 9. However, the passage cited by Rambus' expert does not mention outputting data on the rising and falling edges of an <u>external</u> clock signal.

[29] *See* 37 C.F.R. § 1.104 "In rejecting claims the examiner may rely upon admissions by the applicant, or the patent owner in a reexamination proceeding, as to any matter affecting patentability[.]" *See also,* MPEP § 2217 and 2258(I)(F)("an admission by the patent owner of record in the file or in a court record may be utilized in combination with a patent or printed publication....The admission can reside in the patent file (made of record during the prosecution of the patent application) or may be presented during the pendency of the reexamination proceeding or in litigation.")

B. Invalidity Analysis

The following analysis applies several prior art printed publications that describe synchronous DRAMs to the claims of the '916 patent. Although the Requestor does not believe that these publications would anticipate under properly construed claims, the following analysis is provided in response to Rambus' previous claim construction and infringement allegations in their attempt to cover synchronous DRAMs. Requester does not agree with the claim construction asserted by Rambus in other litigations or with Rambus' infringement allegations, but in the alternative, is hereby asserting that the claims as construed by Rambus are invalid in view of the new prior art references presented herein. By construing the claim language in the manner proffered by Rambus, and/or as otherwise set forth explicitly or implicitly herein, Requester is not admitting and/or acquiescing as to the correctness and/or reasonableness of Rambus' proffered claim construction in the litigation and/or as otherwise set forth herein.

1. Rejections Under 35 U.S.C. §102

The following is a quotation of 35 U.S.C. § 102(b) which forms the basis for all anticipation rejections:

> A person shall be entitled to a patent unless ...
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States

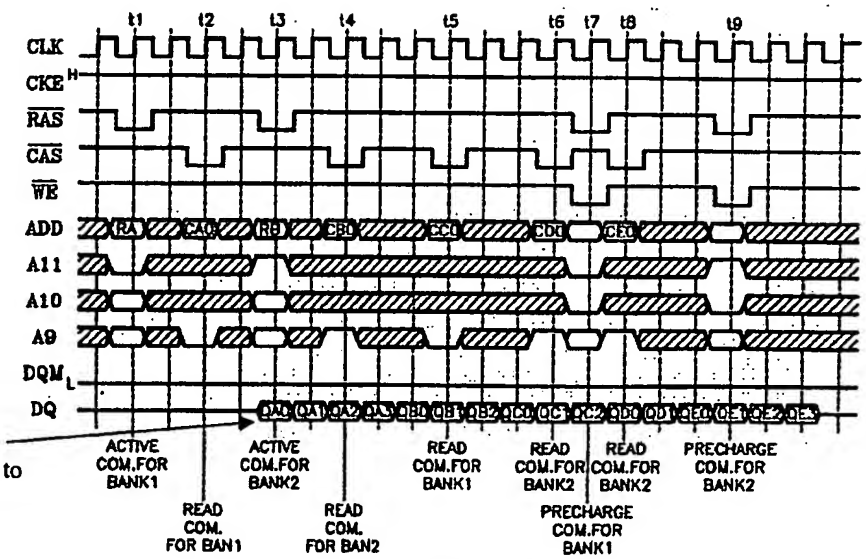
Park

At least claims 1, 2, 4, 5, 10, 12-16, 19, 20, 23, 25-30, 32, 35, 37, 39, and 41 are anticipated by U.S. Patent No. 5,590,086 to Park et al. ("Park", Exhibit B). Claim terms in the following analysis are italicized for the sake of reference.

Independent claims 1, 15, and 26:

1) Regarding claims 1, 15, and 26, Park discloses "a semiconductor memory and, more particularly, a *synchronous dynamic random access memory* which is capable of accessing data in a memory cell array disposed therein in synchronism with a system clock from an external system such as a central processing unit (CPU)." Col. 1, lns. 10-15. For purposes of explanation, the elements of claim 1 and the corresponding anticipatory disclosure in Park are set forth in the claim chart that follows.

Elements of Claim 1	**Park**
receiving a value that is representative of a number of cycles of an external clock signal to transpire after which the memory device responds to a first operation code;	Under Rambus' construction, CAS/ Latency values are within this limitation. "An operation mode set circuit 58 is responsive to the operation mode set command, signals ϕ_{RP}, ϕ_C and ϕ_{WRC} address signals RA0-RA6f so as to set various operation modes, for example, operation modes for establishing a /CAS latency, a burst length representing the number of continuous output data." Col. 13, lns. 3-9. "[A]ddress code register 202" stores CAS latency information in address columns "A6, A5, and A4", as illustrated in Table 1 at col. 18, lns. 41-50.
Receiving block size information, wherein the block size information is representative of an amount of data to be output by the memory device in response to the first operation code;	Under Rambus' construction, control signals specifying an operation are within these claims. "To increase the convenience of use and also enlarge the range of applications, it is more desirable to allow an on-chip synchronous DRAM to not only operate at various frequencies of the system clock, but also be programmed to have various operation modes such as a latency depending on each clock frequency, a burst length or size defining the number of output bits, a column addressing way or type, and so on." Col. 2, lns. 40-47.
sampling the first operation code synchronously with respect to a transition of the external clock signal; and	Under Rambus' construction, control signals specifying an operation are within this limitation. "When the low level /RAS, the high level /CAS and the low level /WE have been sampled at the leading edge of the clock CLK, a precharging operation is performed. An establishment of operation mode set command according to the feature of the present invention is accomplished at low levels of /RAS, /CAS and /WE at the leading edge of clock CLK." Col. 12, lns. 10-16.
Outputting the amount of data, in response to the first operation code, after the number of clock cycles of the external clock signal transpire.	Under Rambus' construction, the function of the device with respect to the CAS/ Latency value is within this limitation. "The 8-bit parallel data continuously outputs every clock cycle thereof." Col. 11, lns. 16-17; see also Figs. 57, 23, 26 Fig. 57, which is reproduced and annotated below, is a timing diagram illustrating a latency between receipt of a read command and the outputting of data on DQ lines.



CAS latency of 2 (2 cycles from t2 to active data)

FIG. 57

Independent claim 26 further requires *clock receiver circuitry*. Fig. 3 of Park shows a row control circuit having a "clock buffer" that receives an external clock signal "CLK." See also Fig. 4 which illustrates various SDRAM components being clocked off a buffered external clock signal, φCLK.

Additional analysis mapping each and every limitation of claims 1, 15, and 26 to Park is provided in the claim chart attached as Exhibit O.

Dependent claims 2, 4, 5, 10, 12-14, 16, 19, 20, 23, 25, 27-30, 32, 35, 37, 39, and 41

2) As to claims 2, 10, 20, 30, and 35, under Rambus' construction, the use of gated non-periodic internal signals derived (no matter how remotely) from an external clock to output data are within these claims. Park teaches a SDRAM with data output drivers for outputting data onto a data bus, as represented in Fig. 26, that receives an input clock signal, φCLK. Fig. 6 shows that the input clock signal φCLK is derived from the external clock CLK. Under Rambus' construction, the data is outputted *synchronously with respect to the external clock signal*, as shown in Fig. 57, reproduced above.

3) As to claims 4 and 16, under Rambus' construction, control signals specifying an operation such as read and write commands are within these claims. Park teaches a SDRAM that performs both read (*first operation code*) and write (*second operation code*) functions. As

illustrated in Fig. 5A, a write command is received when RAS/ is asserted high and CAS/ and WE/ are asserted low, all on the rising edge of the clock signal, CLK. Fig. 54 shows that when a write command is made (t7), a write latency of one is observed.

4) As to claims 5 and 37, under Rambus' construction, addresses received on a separate address bus are within these claims. Fig. 57 reproduced above shows *address information* being sampled *synchronously with respect to the external clock signal*. Figs. 3-4 describe row address and column address decoders for receiving and decoding the *address information* received from address bus to identify *at least one memory cell in the array of memory cells*.

5) As to claim 9, under Rambus' construction, control signals specifying a read command and a portion of the address bus specifying an additional precharge operation is within this claim. Figs. 5a and 5b of Park describe activate, read, write, *precharge*, and refresh operation codes.

6) As to claims 12-14, 19, 23, 25, 27-28, 39, and 41, under Rambus' construction, the use of gated non-periodic internal signals derived (no matter how remotely) from an external clock to sample data, CAS/ Latency values, burst length information received on an address bus and control signals specifying an operation are within these claims. Under Rambus' construction, Park teaches receiving a *binary value* for burst length and CAS latency *synchronously with respect to the external clock signal*. For example, block size information comes in from the address pins, which feed into synchronous circuits. Col. 18, Table 1. Similarly, the CAS/ Latency value is input to address pins A0-A7 (*first input receiver circuitry*). Park also teaches an operation mode set command (*third operation code*) initiated by RAS/, CAS/, and WE/ being asserted low at the external clock edge. See col. 12, lns. 12-18. Further, as shown in Fig. 13, the mode set command ("φMRS") is input to an "Address Code Register" from which "Burst Length Logic" and "Latency Logic" are driven.

7) As to claims 29 and 32, under Rambus' construction, control signals specifying an operation are within these claims. Under Rambus' construction, Park discloses a *first input receiver circuitry* including address pins A0-A7. Under Rambus' construction, Park also discloses a *second input receiver circuitry* including the RAS/, CAS/, and WE/ pins. As illustrated in the timing diagram in Fig. 54, the address and control signals are sampled synchronously with the CLK signal.

Additional and more detailed analysis mapping each and every limitation of claims 1-2, 4-5, 9-10, 12-16, 19-20, 23, 25-30, 32, 35, 37, 39, and 41 to Park is provided in the claim chart attached as Exhibit O.

The JEDEC Standard

At least claims 1-5, 9-10, 12-16, 18-20, 23, 25-27, 30-32, 35, 37, and 40-41 are anticipated by the Joint Electron Device Engineering Council (JEDEC) Standard No. 21-C, Revision 9 published in 1999 ("JEDEC Standard", Exhibit C). Claim terms in the following analysis are italicized for the sake of reference.

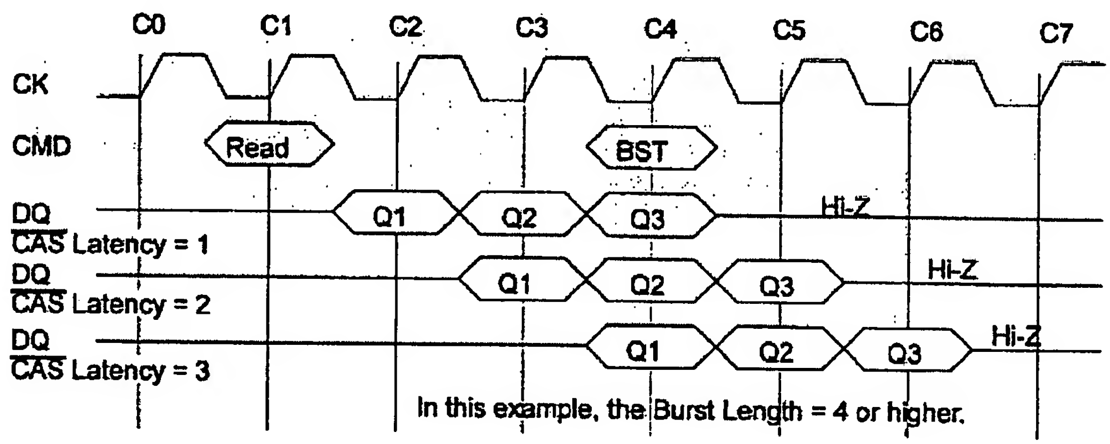
Independent claims 1, 15, and 26:

8) As to claims 1, 15, and 26 the JEDEC Standard provides a standard according to which a compliant *synchronous memory device* must operate. The standard includes pinouts as well as functional requirements and timing diagrams for SDRAMs.

The JEDEC Standard describes each of the limitations recited in independent claims 1, 15, and 26 of the '916 patent. For purposes of explanation, the elements of claim 1 and the corresponding anticipatory disclosure in the JEDEC Standard are set forth in the claim chart that follows.

Elements of Claim 1	**The JEDEC Standard**
receiving a value that is representative of a number of cycles of an external clock signal to transpire after which the memory device responds to a first operation code;	Under Rambus' construction, CAS/ Latency values are within this limitation. "The [mode-of-operation] data contains the Burst Length, the Burst Type, the CAS/ Latency (Defined separately for SDR and DDR devices), and whether [the SDRAM chip] is to be operating in Test Mode, or Normal operating mode." Section 3.11.5.1.3. See also Figure 3.11.5.1-1 showing possible CAS latencies of 2, 3, or 4.
Receiving block size information, wherein the block size information is representative of an amount of data to be output by the memory device in response to the first operation code;	Under Rambus' construction, control signals specifying an operation are within these claims. "The [mode-of-operation] data contains the Burst Length, the Burst Type, the CAS/ Latency (Defined separately for SDR and DDR devices), and whether [the SDRAM chip] is to be operating in Test Mode, or Normal operating mode." Section 3.11.5.1.3. Desired burst length value is determined from Bit 2:0 of

Elements of Claim 1	The JEDEC Standard
	the mode-of-operation opcode. Figure 3.11.5.1-1.
Sampling the first operation code synchronously with respect to a transition of the external clock signal; and	Under Rambus' construction, control signals specifying a read operation are within this limitation. The first operation code is a read command. Section 3.11.5.1.16 A "Read" CMD is sampled during transition of the external clock signal CK. See the timing diagram at section 3.11.5.1.16
outputting the amount of data, in response to the first operation code, after the number of clock cycles of the external clock signal transpire.	Under Rambus' construction, the function of the device with respect to the CAS/ Latency value is within this limitation. See pg. 3.11.5.1-17, Figure -1 reproduced below which shows data being outputted after a CAS latency of 1, 2, and 3.



Independent claim 26 further requires *clock receiver circuitry*. This claim limitation is also met, as shown in the block diagram of Fig. 1, with respect to the clock signal CLK. Specifically, external clock signal CLK is received at an input pin in a memory device. See Fig. 3.11.3-2, pin #38.

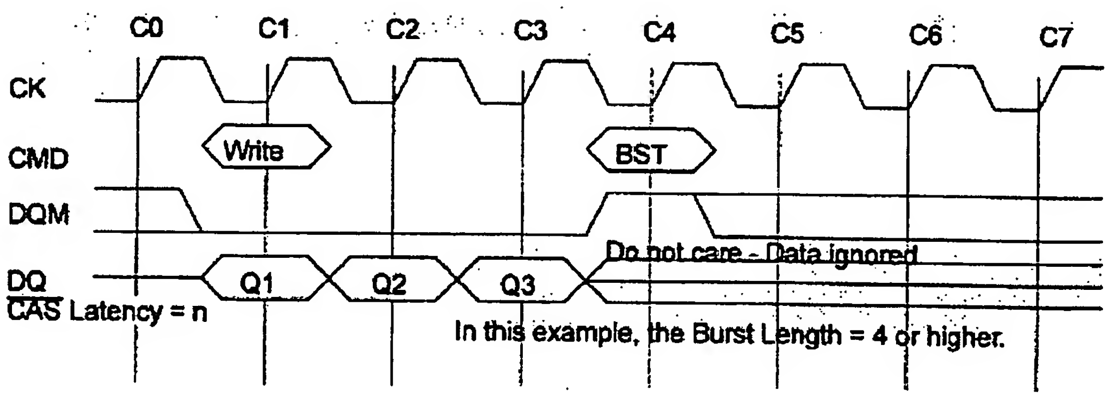
Additional and more detailed analysis mapping the JEDEC Standard to each and every limitation of claims 1, 15, and 26 of the '916 patent is provided in the claim chart attached as Exhibit P.

Dependent claims 2-5, 9-10, 12-14, 16, 18-20, 23, 25, 27-32, 35, 37, and 39-41:

9) As to claims 2, 10, 20, 30, and 35, under Rambus' construction, the use of gated non-periodic internal signals derived (no matter how remotely) from an external clock to output data are within these claims. Under Rambus' construction, the JEDEC Standard, as shown in the timing diagram above, discloses the outputting of data *synchronously with respect to an external clock signal.* In this regard, the JEDEC Standard discloses that "[d]uring reads, DQM performs synchronous output enable." Pg. 3.11.5.1.10. Thus, "[f]or reads, DQM latency is defined as the difference between the clock when DQM is asserted and the clock when the output bus has been forced to High-Z." Pg. 3.11.4.1.10. Accordingly, under Rambus' construction, the JEDEC Standard discloses the output of data *synchronously with respect to an external clock signal.*

10) As for claims 3, 18, and 31, under Rambus' construction, the use of gated non-periodic internal signals derived (no matter how remotely) from an external clock to output data are within these claims. The JEDEC Standard also discloses operational information for double or dual data rate (DDR) operation of a SDRAM, which, under Rambus' construction, inputs or outputs data *synchronously with respect to a rising edge transition [and] falling edge transition of the external clock signal.* Specifically, the JEDEC Standard teaches that, "Driven by the DDR SDRAM during output of Read data, and Driven by the Memory Controller during input of Write data, the rising and falling edges of that signal (DQS) will indicate the output of Read Data and the input of Write Data on the data output and input pins (DQ) of DDR SDRAM." Pg. 3.11.5.2.1.

11) As to claims 4 and 16, under Rambus' construction, control signals specifying an operation such as read and write are within these claims. The JEDEC Standard discloses that the SDRAM performs both read and write functions. See Table 3.11.4.1-1 (SDRAM Function Truth Table). As such, the SDRAM is functional with a read command (*first operation code*) and a write command (*second operation code*). As shown in the timing diagram below, a write request is sampled *synchronously* with respect to *an external clock signal* and data is input on the DQ pins in response to the write command.

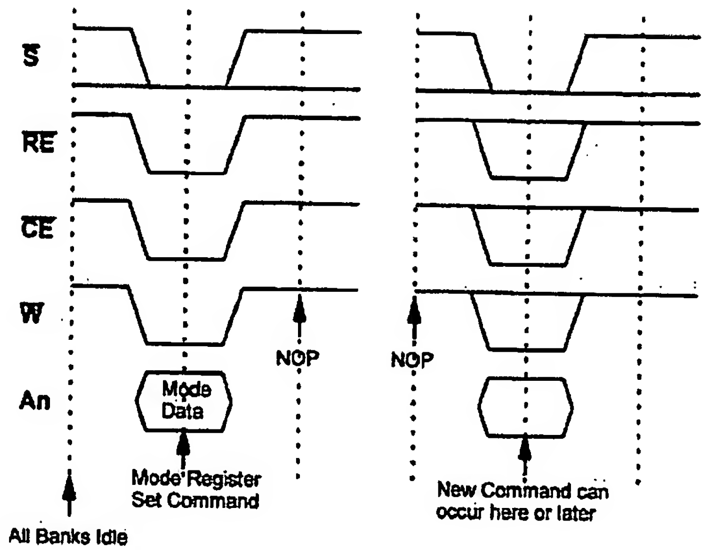


Further, as noted in the timing diagram, the write request is executed with a burst length (*block size information*) of four that has been interrupted with a burst terminate command (BST).

12) As to claims 5 and 37, under Rambus' construction, addresses received on a separate address bus are within these claims. The SDRAM Function Truth Table, pg. 3.11.5.1.1, shows general SDRAM functions, including, receiving an address identifying *at least one memory cell in the array of memory cells.* In addition, the address information is received synchronously with respect to the external clock. Sections 3.11.5.1.9 and 3.11.5.1.12 illustrate that the address information is sampled with respect to the external clock.

13) Regarding claim 9, under Rambus' construction, control signals specifying a read command and a portion of the address bus specifying an additional precharge operation is within this claim. The JEDEC Standard discloses that the SDRAM may execute a read command with or without a *precharge* operation. Specifically, an address bit (AP) during a column address cycle of a read command indicates whether a precharge will be utilized. See also Table 3.11.5.1-1 (SDRAM Function Truth Table).

14) As to claims 12-14, 19, 25, 27-28, 39, and 41, under Rambus' construction, the use of gated non-periodic internal signals derived (no matter how remotely) from an external clock to sample data, CAS/ Latency values, and control signals specifying an operation are within these claims. The JEDEC Standard teaches receiving a *binary value* for burst length and CAS latency *synchronously with respect to the external clock signal.* This is further shown at section 3.11.5.1.7 in the figure reproduced below.



15) As to claims 13, 25, 39, and 41, CAS/ Latency values, and control signals specifying an operation are within these claims. The data provided to the mode set register during a mode set operation includes burst length and CAS/ latency information that is in the form of bit values at bits b0-b2 and b4-b6, respectively. Under Rambus' construction, the values at these respective bit locations therefore constitute *a binary code* for signaling *block size information and a CAS/ Latency value.*

16) As to claim 23, under Rambus' construction, control signals specifying an operation and burst length information on an address bus are within these claims. The JEDEC Standard teaches that a read command (*first operation code*) is identified by states on S/, RE/, CE/, and W/ on a control bus, as set forth in the JEDEC SDRAM Function Truth Table on page 3.11.5-3. Under Rambus' construction, block size information is provided on an address bus.

17) With regard to claims 29 and 32, under Rambus' construction, control signals specifying an operation are within these claims. The JEDEC Standard teaches a programmable timing and control register that reads the inputs on WEB, CASB, and RASB to sample a write request (*second operation code*). Section 3.11.5.1.7. Under Rambus' construction, the JEDEC Standard *samples a second operation code with respect to an external clock.*

18) As to claim 40, the JEDEC Standard discloses *delay lock loop circuitry.* Specifically, "[t]he edges of the Output Data pins, DQ, and the edges of the Data Strobe (pins), DQS, during a read are nominally coincident with the edges of the input clock. This is

accomplished by an internal DLL or similar circuitry." Pg. 3.11.6-11. Moreover, "the output data drivers and data strobe driver(s) are driven by the same clock minimizing the skew between DQS and DQ." Pg. 3.11.6-12.

A claim chart that provides specific and detailed applicability of the reference to each and every limitation of claims 1-5, 9-10, 12-16, 18-20, 23, 25-27, 30-32, 35, 37, and 39-41 is attached as Exhibit P.

Hynix

19) At least claims 1, 3, 9, 12, 14, 26, 28, 31, and 37 are anticipated by the Hyundai HY5DV651622 data sheet, Rev. 0.9, published January 2000 ("Hynix -1," Exhibit D, Tab 1). In the Hynix Litigation, Rambus accused the Hynix HY5DV651622 of infringing the above-listed claims.[30] Rambus has provided a claim chart that allegedly maps the elements of claims 1, 3, 9, 12, 14, 26, 28, 31, and 37 to the accused device. See Exhibit AI, Tab 3.

Under Rambus' own interpretations of the '916 patent claims, Hynix -1 anticipates at least claims 1, 3, 9, 12, 14, 26, 28, 31, and 37 of the '916 patent.

2. Rejections Under 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis of all obviousness rejections:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

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[30] See Rambus Inc.'s Final Infringement Contentions at pgs. 1, 2, Exhibit AI, Tab 1. In the Hynix Litigation, Rambus asserts that the Hynix HY5DU28822T is "representative" of all the accused DDR SDRAM devices, which includes the Hynix HY5DV651622. The list of accused devices is provided in Exhibit AI, Tab 2 (Exhibit A to Rambus Inc.'s Final Infringement Contentions). The data sheet for the Hynix HY5DU28822T is provided in Exhibit AI, Tab 4 (Exhibit R to Rambus Inc.'s Final Infringement Contentions).

Also, Rambus was limited to 65 asserted claims by the Court. Rambus indicated that the list of claims in its contentions "is not a comprehensive list of the claims infringed by Hynix." Exhibit AI, Tab 1, pg. 1.

Park in view of the JEDEC Standard

20) Claims 3, 18, 31, and 40 are rendered obvious based on Park in view of the JEDEC Standard. Under Rambus' construction, the use of gated non-periodic internal signals derived (no matter how remotely) from an external clock to output data is within these claims. The JEDEC Standard specifies a DDR (Doubled Data Rate) SDRAM whereby "the rising and falling edges of that signal (DQS) will indicate the output of Read Data and the input of Write Data on the data output and input pins (DQ) of DDR SDRAM." Section 3.11.5.2-2. Under Rambus' construction, the JEDEC Standard also describes *delay lock loop circuitry* for SDRAMs. Specifically, the JEDEC Standard provides that "[t]he edges of the Output Data pins, DQ, and the edges of the Data Strobe pin(s), DQS, during a read are nominally coincident with the edges of the input clock. This is accomplished by an internal DLL or similar circuitry." Section 3.11.6-11.

The JEDEC Standard provides the motivation to combine the two references. As the standardizing body, JEDEC, in the draft 21-C standard, by definition, suggests the design standards that are to be adopted for all compliant SDRAM designs. Thus, one skilled in the art would have been motivated to incorporate the design specifications from the draft JEDEC Standard into the SDRAM described by Park so that when the specification was finally adopted, the device would be JEDEC compliant.

Hynix -1 in view of Hynix -2 and Hynix -3

21) At least claims 1, 3, 9, 12, 14, 26, 28, 31, and 37 are anticipated by the Hyundai, HY5DV651622, Rev. 0.9 ("Hynix -1," Exhibit D, Tab 1) in view of Hyundai, SDRAM Timing Diagram, Rev. 1.2 ("Hynix -2," Exhibit D, Tab 2) and Hyundai, DDR SDRAM DEVICE OPERATION, Rev. 0.2 ("Hynix -3," Exhibit D, Tab 3). The analysis referenced in paragraph 19) above describes why each and every limitation of these claims is described in at least one of these references.

Motivation to combine these references exists because they are discussing the *same family of devices*. Furthermore, one of ordinary skill in the art would naturally look to the additional references describing Hynix's SDRAM products to better understand the details being discussed in Hynix -1.

SECTION TWO:
Rejection Of Claims 1-41 In View Of Publications Prior To April 18, 1990

The '916 patent belongs to a 10+ year patent family comprising multiple patents and patent applications dating back to the original '898 application filed on April 18, 1990. As discussed in section one above, claims 1-5, 9-10, 12-20, 23, 25-32, 34-35, 37, and 39-41 of the '916 patent are not entitled to a claim of priority to the original '898 application. However, as discussed in more detail below, these and the remaining claims of the '916 patent are also invalid over multiple prior art references that are prior art to April 18, 1990, the earliest possible priority date of the '916 patent.

A. Rejections Under 35 U.S.C. §102

The following is a quotation of 35 U.S.C. § 102(b) which forms the basis for all anticipation rejections:

> A person shall be entitled to a patent unless ...
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States.

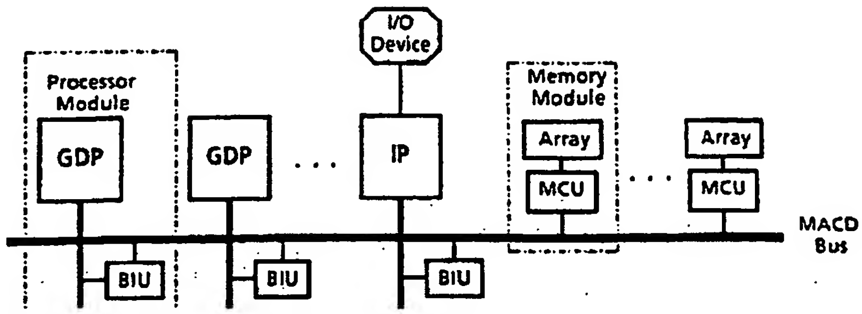
There are a group of publications that similarly describe the Intel iAPX system. For the sake of convenience, two of these references are discussed below: the iAPX Manual, which is a reference manual published by Intel, and Budde, which is a U.S. patent assigned to Intel.

<u>Intel iAPX Manual</u>

At least claims 1-2, 4-8, 10-17, 19-26, 28-30, 32-39, and 41 of the '916 patent, as construed by Rambus, are anticipated by <u>iAPX 432 Interconnect Architecture Reference Manual</u>, published in 1982 ("the iAPX Manual", Exhibit E, Tab 1). Claim terms in the following analysis are italicized for the sake of reference.

Independent claims 1, 15, and 26:

22) Independent claims 1, 15, and 26 of the '916 patent are anticipated by the iAPX Manual. Specifically, the iAPX Manual describes a memory module (*memory device*) that is formed by the combination of a memory control unit (MCU) and its associated storage array, as illustrated in the portion of Figure 1-2 reproduced below. Pg. 1-3.



The memory module is connected to a processor module and other devices across an external bus, referred to as the memory bus or "MACD Bus," as shown above in Fig. 1-2 at pg. 1-3. The memory module is *synchronous*, as illustrated by two clock inputs – CLKA and CLKB. See Table 5-6, pg. 5-21.

Additionally, the iAPX Manual describes each of the limitations recited in independent claims 1, 15, and 26 of the '916 patent. For purposes of explanation, the elements of claim 1 and the corresponding anticipatory disclosure in the iAPX Manual are set forth in the claim chart that follows.

Elements of Claim 1	**The iAPX Manual**
receiving a value that is representative of a number of cycles of an external clock signal to transpire after which the memory device responds to a first operation code;	During an initialization cycle, the MCU receives a value "s", that indicates a number of clock cycles to transpire before the memory responds to a read request. The MCU includes an INIT/ input for starting an initialization cycle. Pgs. 5-21. "The initialization data is loaded from the memory bus and the ACD or SLAD bus while the INIT signal is asserted." Pg. 9-7. In the second phase of the initialization (D2) the "s" (Array Speed) parameter is acquired from the SLAD bus and loaded in MCU register 01. Pgs. C-2, C-7, D-4, D-5. "The s field indicates the characteristics that the MCU is to use when accessing the external memory array. The s field indicates whether the MCU will access the storage array with nominal (c-1) or extended (c-0) access time. Extended access time lengthens the nominal access time by one component clock cycle." Pg. C-8. The first operation code is a "memory read request." Pg. F-5.
receiving block size information, wherein the block size information is representative of an amount of	Bits [11:8] of a "Memory Read Request" are referred to as the "LLLL" field. Pg. F-5, Table F-1. "The LLLL field indicates the number of bytes of memory data to be transferred by a memory access. The encoding of the

Elements of Claim 1	The iAPX Manual
data to be output by the memory device in response to the first operation code;	LLLL field follows: LLLL Memory Access Length 0000 1 byte 0001 2 bytes 0010 3 bytes ... 1111 16 bytes" Pg. F-3.
sampling the first operation code synchronously with respect to a transition of the external clock signal; and	The MCU is a synchronous device that communicates over the memory (MACD) bus using message packets, including a Memory Read Request message. Pg. F-2 and F-5. "The memory requests are issued to a memory bus as packets of information." Pg. 1-5. The MCU includes two clock inputs: CLKA and CLKB. Pg. 5-21, Table 5-6. When the operation code bits [15:12] of a message packet are set to "0000", this specifies that the requested operation is a Memory Read Request message packet. Pg. F-5. These bits are sampled in the first bus cycle (T=0). Pg. F-5. In one example, the memory bus operates at a clock speed of 5 MHz. Pg. C-25.
outputting the amount of data, in response to the first operation code, after the number of clock cycles of the external clock signal transpire.	The MCU outputs data in a "Memory Bus Reply Message", as shown in Table F-2. Pg. F-6. The timing for the reply message to a read request is set during the initialization cycle, discussed above. The MCU has a programmable delay (measured in clock cycles) for accessing the memory array, and would therefore be delayed in providing its reply message accordingly. (See pg. C-8: "The s field indicates whether the MCU will access the storage array with nominal (c=1) or extended (c=0) access time. Extended access time lengthens the nominal access time by one component clock cycle.")

Independent claim 26 further requires *clock receiver circuitry*. This claim limitation is also met, as discussed above with respect to the clock inputs CLKA and CLKB, which are received at two pins on the MCU. Table 5-6.

A complete and more detailed claim chart mapping the iAPX Manual to the limitations of claims 1, 15, and 26 is attached hereto as Exhibit Q.

Dependent claims 2, 4-8, 10-14, 16-17, 19-25, 28-30, 32-39, and 41

23) As to dependent claims 2, 10, and 30, the iAPX Manual teaches that the Reply Message outputting data from the memory module is *synchronous* since it is packetized on the clocked memory bus. See Table F-2 at pg. F-6.

24) As to dependent claims 4 and 16, the iAPX Manual teaches that the synchronous memory module performs both read (*first operation code*) and write (*second operation code*) transactions. Specifically, a "Memory Write Request" is *a second operation code* that is provided to the memory module during a first clock cycle (T=0). Pg. F-5. Table F-1, reproduced below, shows the format for message packets sent on the memory bus. As stated above, the memory bus is a *synchronous* bus and includes two clock signals CLKA and CLKB. Pgs. 5-21 and C-25.

Table F-1. Memory Bus Request Message Formats

CCC 2 0	Upper MACD Byte 15 8	Lower MACD Byte 7 0	T	Request Message
000 001	0000LLLL MADRB(1)	MADRB(2) MADRB(0)	0 1	Memory Read Request
000 001	0001LLLL MADRB(1)	MADRB(2) MADRB(0)	0 1	Memory RMW Read Request
001 001 001 • • 000 001	0010LLLL MADRB(1) DATAB(1) • • DATAB(N-3) DATAB(N-1)	MADRB(2) MADRB(0) DATAB(0) • • DATAB(N-4) DATAB(N-2)	0 1 2 • • C-2 C-1	Memory Write Request
001 001 001 • • 000 001	0011LLLL MADRB(1) DATAB(1) • • DATAB(N-3) DATAB(N-1)	MADRB(2) MADRB(0) DATAB(0) • • DATAB(N-4) DATAB(N-2)	0 1 2 • • C-2 C-1	Memory RMW Write Request
000 001	0100000B IADRB(1)	IADRB(2) IADRB(0)	0 1	Interconnect Read Request
001 000 001	0101000B IADRB(1) DATAB(1)	IADRB(2) IADRB(0) DATAB(0)	0 1 2	Interconnect Write Request

Responsive to a write request, the memory device inputs variably-sized data from the memory (MACD) bus and does so *synchronously* with respect to *an external clock signal*. "The MCU accepts variable length data requests from the memory bus and performs the necessary accessing to read or write the data into the storage array." Pg. 1-4. As shown in the table above, for a memory write request, a variable amount ("N") of data is input by the memory device for a Memory Write Request.

25) As to dependent claims 5-8, 11, 21-24, 34, and 36-38, the iAPX Manual teaches a *synchronous*, *multiplexed*, and *packet* communication protocol including *address information*, control (e.g., *operation code, block size*), and data received over the signal lines of a *bus*, which is external to the memory module. "Memory requests are issued to a memory bus as packets of information." Pg. 1-5. Address information, control information and data are sampled synchronously from the MACD bus with respect to an external clock signal. Col. 7, lns. 11-19. According to the message format tables, the memory (MACD) bus is two bytes (16 bits) wide. Pgs. F-5 through F-6. Information from the bus is received on input pins in the MCU. Table 5-6.

26) As to dependent claims 12-13, 25, 39, and 41, the "LLLL" field and the "s" field represent *block size information* and *a number of cycles of the external clock signal to transpire after which the memory device responds*, respectively. The bit value of the "s" field and the bit values in the "LLLL" are in *binary code*. See Table 1, reproduced above. The *block size information*, like other informed received from the MACD bus, is sampled *synchronously with respect to an external clock.* Pg. F-5.

27) As to dependent claims 14, 19, and 28, the iAPX Manual discloses an INIT/ signal (*operation code*) that is received to start an initiation cycle in which the MCU stores the value "s" into the MCU register 01. See pg. C-7 through C-8.

28) As to dependent claim 17, to the extent Rambus asserts that this claim covers any delay between the receipt of an op code and the sampling of data, as described above, the data will be sampled after a *delay time* transpires because the address, control, and data are multiplexed in a packet. Specifically, in the message format for a Memory Write Request, the address and length are provided in the first two cycles (T) of the message, and the data to be written is provided in the following cycle(s). As such, data that is to be input is not sampled until a certain period after a number of clock cycles.[31]

29) As to dependent claims 20 and 35, as previously shown, the MACD bus receives data from the memory module in response to a read request (*first operation code*). In this regard,

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[31] It is noted that claim 17 uses the term *delay time*, which is distinguished from claim 1 which refers to *a value that is representative of a number of cycles of an external clock signal to transpire after which the memory device responds to a first operation code.*

the iAPX Manual discloses *receiving the amount of data output by the memory device.* This data is driven onto the MACD bus by output drivers, as discussed above.

30) As to dependent claims 29, 32, and 34, under Rambus' construction, a set of control lines can be both a first and a second input receiver circuitry. The iAPX Manual describes *input receiver circuitry* that receives message packets. The message packets provide all information including address, data, and control over a single bus.

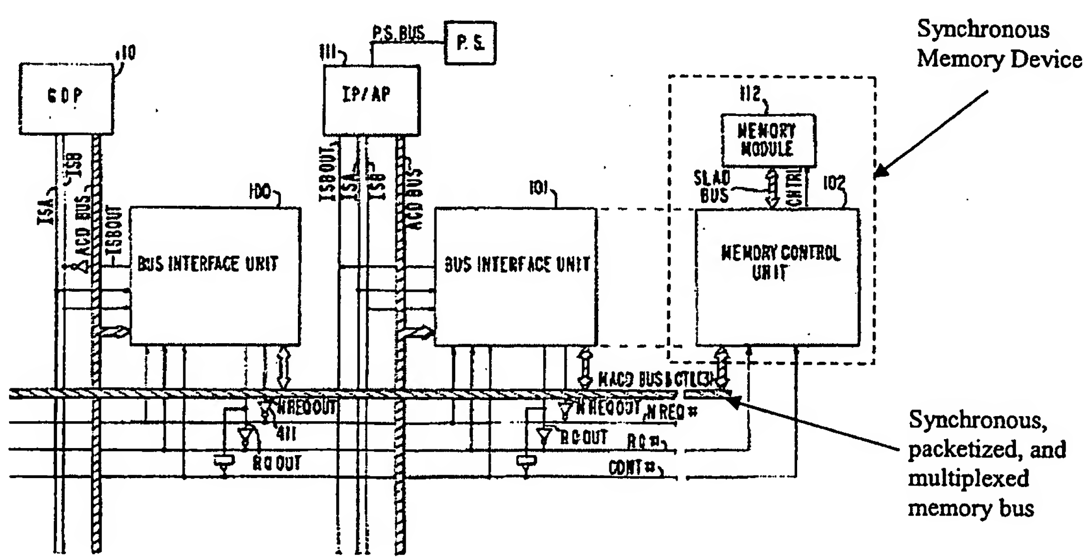
A complete and more detailed claim chart mapping the iAPX Manual to the limitations of claims 1-2, 4-8, 10-17, 19-26, 28-30, 32-39, and 41 is attached hereto as Exhibit Q.

Budde

At least claims 1-2, 4-8, 10-17, 19-30, 32-39, and 41 of the '916 patent are anticipated by Budde et al., U.S. Patent No. 4,480,307 ("Budde"), a copy of which is attached at Exhibit F. Claim terms in the following analysis are italicized for the sake of reference.

Independent claims 1, 15, and 26:

31) Independent claims 1, 15, and 26 each call for a *synchronous memory device* that includes an array or plurality of *memory cells.* Budde discloses a "memory control unit 102" and a "memory module 112" connected to one another by a "SLAD bus" and a "CNTRL bus" that collectively form a *synchronous* memory device, as shown in Figure 1 reproduced below. Figure 1 is annotated to include a box around the memory module 112 and the memory control unit 102.



Budde teaches that "[t]he MCU receives variable-length access requests at its memory bus interface from a bus interface unit on the MACD bus and makes the proper series of accesses to memory through its storage bus interface. After completion of the accesses to memory, the MCU returns the proper reply on the MACD bus." Col. 9, lns. 46-54. Additionally, the memory device is *synchronous* as "CLKA and CLKB provide basic timing references for the BIU and MCU. CLKB lags CLKA by (nominally) 1/4 cycle (90 degrees). Arbitration related signals are driven with CLKA falling, and sampled with CLKA falling. MACD [15:0] is driven and sampled with CLKB rising (3/4 cycle timing). Buffer directional control for the memory bus is altered with CLKA rising." Col. 7, lns. 11-19. Furthermore, the memory device disclosed by Budde comprises an array of memory cells as "[t]he MCU is connected to a single bank, 40-bit wide, ECC corrected dynamic RAM storage array with spare bit." Col. 10, lns. 30-31.

Additionally, Budde describes each of the limitations recited in independent claims 1, 15, and 26 of the '916 patent. For purposes of explanation, the elements of claim 1 and the corresponding anticipatory disclosure in Budde are set forth in the claim chart that follows.

Elements of Claim 1	**Budde**
receiving a value that is representative of a number of cycles of an external clock signal to transpire after which the memory device responds to a first operation code;	The value of the number of clock cycles the memory device waits before outputting data in response to a read request ("first operation code") is set during initialization or "INIT" time of the MACD memory device. Specifically, memory read data is received "in two clock cycles, and follows the outgoing address by a <u>specified number of clock cycles</u>. The number of clocks to wait is specified at "INIT" time as the memory access time." Col. 10, lns. 48-52 (emphasis added).
receiving block size information, wherein the block size information is representative of an amount of data to be output by the memory device in response to the first operation code;	The "MCU receives variable length access requests at its memory bus interface from a bus interface unit on the MACD bus and makes the proper series of accesses to memory through its storage bus interface. After completion of the accesses to memory, the MCU returns the proper reply on the MACD bus." Col. 9, lns. 47-54. Thus, when a memory access is detected, a bus interface unit will "issue a memory bus access, with appropriate address and length." Col. 18, lns. 19-20. Budde further identifies that such an access, e.g., a memory read request, is encoded as "0000LLLL HADR, LADR." Col. 12, ln. 33. The value "LLLL" is the length (or amount) of data requested. See Col. 18, lns. 19-21.

Elements of Claim 1	**Budde**
	See also U.S. Pat. No. 4,315,308 (Exhibit G) which describes that the "LLLL" value in a packet specifies the number of bytes to be provided.[32]
sampling the first operation code synchronously with respect to a transition of the external clock signal; and	The MACD bus, which receives operation codes as part of a request packet [15:0], is driven and sampled with CLKB rising. Col. 7, lns. 11-19.
outputting the amount of data, in response to the first operation code, after the number of clock cycles of the external clock signal transpire.	"Memory read data is received by the MCU on the SLAD bus in two clock cycles, and follows the outgoing address by a <u>specified number of clock cycles</u>. The number of clocks to wait is specified at "INIT" time as the memory access time." Col. 10, lns. 47-52 (emphasis added). "After completion of the accesses to memory, the MCU returns the proper reply on the MACD bus." Col. 9, lns. 52-54.

Independent claim 26 further requires *clock receiver circuitry*. This claim limitation is also met, as discussed above with respect to the clock signals CLKA and CLKB.

Additional and more detailed analysis mapping Budde to each and every limitation of claims 1, 15, and 26 of the '916 patent is provided in the claim chart attached as Exhibit R.

Dependent claims 2, 4-8, 10-14, 16-17, 19-25, 27-30, 32-39, and 41

32) As for dependent claims 2, 10, 20, 30, and 35 of the '916 patent, Budde teaches a memory device outputting data *synchronously with respect to an external clock signal* onto the MACD bus. "Typical operation involves time-multiplexing data on these lines in the following order: Control information for bus transactions, Address information for bus transactions, Data requested by the preceding address and control." Col. 6, 43-47. Two external clocks, CLKA and CLKB, provide clocking for said operation. "MACD [15:0] is driven and sampled with CLKB rising (3/4 cycle timing). Buffer directional control for the memory bus is altered with CLKA rising." Col. 7, lns. 11-19. Output drivers for driving data onto the MACD bus are shown in Fig. 3.

[32] Budde refers to the '308 patent as describing the same system. Col. 3, lns. 50-54. It is proper to refer to multiple references in an anticipation argument if the secondary reference is used to "(B) Explain the meaning of a term used in the primary reference." MPEP § 2131.01.

33) As for dependent claims 4 and 16, Budde teaches a packetized communication system that includes "opcode, address, data, and control" information. Abstract. Moreover, those packets can be "[w]rite-request packets and read-request packets." Abstract. Budde teaches that a "Memory Write Request" may be encoded in a manner similar to a memory read request. Specifically, a memory write request is coded as

"0010LLLL HADR, LADR, D0[,..., Dn]."

Col. 12, lns. 54-55. As previously shown, "LLLL" is a length value representative *of the amount of data to be input by the memory device* in response to a write request. Also, as explained above, Budde teaches that "[t]he MCU receives variable-length access requests at its memory bus interface from a bus interface unit on the MACD bus and makes the proper series of accesses to memory through its storage bus interface." Col. 9, lns. 48-52. In this regard, like a read request, a write request (*second operation code*) is received *synchronously with respect to an external clock signal.*

34) As for dependent claims 5 and 37, as shown in the Read Request packet described above, the memory bus includes "[a]ddress information for the operation requested." Col. 18, lns. 19-21 and col. 6, lns. 40-26. Like the rest of the information in a read request, the address information is sampled *synchronously with respect to an external clock signal.* Col. 7, lns. 11-19.

35) As for dependent claims 6-8, 11, 21-24, 33, 36, and 38, Budde teaches:

> Typical operation involves time-<u>multiplexing</u> data on these lines in the following order:
> Control information for bus transactions,
> <u>Address information</u> for the operation requested,
> Data requested by the preceding address and control.

Col. 6, lns. 43-48, (emphasis added). "Write request-packets and read-packets [that] are issued to the memory-control unit." Abstract. In this regard, each write-request and read-request "packet includes an opcode, address, data, control, and parity-check bits." Abstract. The packets are carried over the MACD bus, which is a 16 bit bus external to the memory device. "MACD (15:0)-16 bits of multiplexed data, address and control." Col. 4, lns. 34-35; Fig. 1.

36) As for dependent claim 12, as set forth above, *block size information* is part of a memory read request ("0000<u>LLLL</u> HADR, LADR," emphasis added). Like the rest of the

information in a memory read request, block size information is sampled *synchronously with respect to a transition of the external clock signal.*

37) As for dependent claims 13, 25, and 41, Budde teaches that read memory requests and write memory requests are encoded as "0000LLLL HADR, LADR" and "0010LLLL HADR, LADR, D0[,..., Dn]," respectively. Thus, "LLLL" is *a 4 bit binary code*. The definition of "LLLL" is further described in U.S. Pat. No. 4,315,308, Fig. 3 (Exhibit G).[33]

38). As for claims 14, 19, 27, 28, and 39, Budde teaches that, in response to an INIT/ signal, the MCU receives initialization parameters including an access time value from the SLAD bus. "The SLAD bus is also used at INIT time to enter into the MCU all memory bus independent initialization parameters. These are: ...memory access time in clock cycles...." Col. 10, ln. 66–col. 11, ln. 6. The access time value is stored in the MCU for later use in responding to read requests. "The number of clocks to wait [when responding to a read request] is specified at 'INIT' time as the memory access time." Col. 10, lns. 47-52.

39) As for dependent claim 17, because the address, control, and data are multiplexed in a packet, as described above, the data will be sampled after a *delay time* transpires. Specifically, in the message format for a Memory Write Request, the control, length, and address HADR information are provided in a first cycle, followed by address LADR and data D0 ... Dn in subsequent cycles. Col. 12, lns. 53-55. As such, to the extent Rambus asserts that this claim covers any type of delay between the receipt of the op code and the sampling of data that is to be input is not sampled until a number of cycles have transpired.[34]

40) As for dependent claims 29 and 34, under Rambus' construction, a set of control lines can be both a first and a second input receiver circuitry. Budde describes a single *input receiver circuitry* that receives message packets over an external bus. The message packets provide all information including address, data, and control.

A claim chart that provides specific and detailed applicability of Budde to each and every limitation of claims 1-2, 4-8, 10-13, 15-17, 20-26, 29-30, 32-39, and 41 is attached as Exhibit R.

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33 Budde cross-references the '308 patent at col. 1, ln. 14. It is proper to refer to multiple references in an anticipation argument if the secondary reference is used to "(B) Explain the meaning of a term used in the primary reference." MPEP § 2131.01.

34 It is noted that claim 17 uses the term *delay time*, which is distinguished from claim 1 which refers to *a value that is representative of a number of cycles of an external clock signal to transpire after which the memory device responds to a first operation code.*

B. Rejections Under 35 U.S.C. §103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis of all obviousness rejections:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

<u>The iAPX Manual in view of the iAPX Specification, Budde and the '308 patent</u>

41) Claims 1-2, 4-8, 10-17, 19-26, 28-30, 32-39, and 41 are identified above as being anticipated by the iAPX Manual and/or Budde. In the alternative to the anticipation arguments provided above, Requester submits that these claims are rendered obvious by the combination of the iAPX Manual, the iAPX Specification, Budde, and the '308 patent (Exhibits D, E, F, and G, respectively). The analysis above describes why each and every limitation of these claims is described in at least one of these references.

Motivation to combine these references exists because they are discussing the *same system*. Furthermore, one of ordinary skill in the art would naturally look to the additional references describing the system to better understand the details being discussed in the iAPX Manual.

<u>The iAPX Manual in view of Rau</u>

42) In the alternative to the anticipation arguments provided above with respect to claims 1, 14, 15, 19, and 26-28, Requester submits that these claims are rendered obvious by the iAPX Manual in view of <u>The Cydra 5 Departmental Supercomputer Design Philosophies, Decisions, and Tradeoffs</u> published in January 1989 by Rau et al ("Rau", Exhibit H). Furthermore, claims 2, 4-8, 10-13, 16-17, 20-25, 29-30, 32-39, and 41 depend on these claims, and are further rendered obvious. Following the claim analysis below is a discussion of the motivation to combine these two references.

Regarding claims 1, 14, 15, 19, and 26-28, the iAPX Manual describes receiving a value "s" that indicates a number of clock cycles to transpire before the memory can respond to a read

request and a register for storing such a latency value. Rau similarly teaches that this value can be provided by an attached numeric processor, Specifically, Rau teaches a memory system that includes a "memory latency register" (MLR) that receives a "value of the memory latency" from a numeric processor. Pgs. 31, 33. The memory system will buffer any output data being read from the memory system for the number of "numeric processor cycles" stored in the memory latency register. Pg. 33. "The MLR allows the compiler to treat memory accesses as having a deterministic latency but to use different values for the latency in different portions of the code so as to always deliver near-optimal performance." Pg. 33.

As for claims 28, 30, 32-39, and 41, as set forth in the anticipation arguments provided above, the iAPX Manual describes the additional limitations in these claims.

One skilled in the art would be motivated to combine the iAPX Manual and Rau based on the teachings of Rau and due to the nature of the problem to be solved. Both the iAPX Manual and Rau are directed to computer and memory systems connected by a common bus, and modifying the interface there between. The iAPX Manual recognizes the problem that memory latency needs to be modified for different reasons (including not wanting to limit the system to the longest contemplated latency), and therefore provides an initialization procedure which provides a *value representative of a number of clock cycles to transpire before responding to the memory request*. Rau recognizes this same problem, but further specifically recognizes that having the processor set the value for the memory latency provides "near-optimal performance." Pg. 33. Upon reviewing Rau and the identified benefits of having the processor set the memory latency value to a minimum value based on the particular type of code that is executing, one skilled in the art would have been motivated to combine the teachings of the iAPX Manual and Rau to provide the memory latency from an external source.[35]

In addition, the iAPX Manual describes a stated desire to provide "flexibility." Pg. 1-2. Furthermore, the iAPX Manual teaches that "[a]ll types of DRAMs are supported: 16K, 64K, 256K, even partially good components." Pg. 1-4. However, in order to achieve this flexibility, "[a] modest amount of external logic is required to interface the MCU to the storage array RAMs[.]" Id. Rau comments about a similar system with a memory latency value provided

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[35] See MPEP § 2143.01 which describes how a motivation to combine references exists when "each reference was directed 'to precisely the same problem.'" Citing *Ruiz v. A.B. Chance Co.*, 357 F.3d 1270 (Fed. Cir. 2004).

from a hardware/hardwired solution: "This made us nervous about hardwiring the nominal memory latency value into the compiler and the hardware." Pg. 33. As a result, Rau proposed a modification to such systems by having the memory latency value being provided from the processor. Thus, upon reading Rau, one of ordinary skill in the art would be motivated to modify the teachings of the iAPX Manual to similarly have the memory latency value provided by the processor.

A reasonable expectation of success exists because the iAPX Manual already describes providing various types of control information over the external MACD bus during the same initialization cycle, and also describes providing a value for memory latency to the MCU.

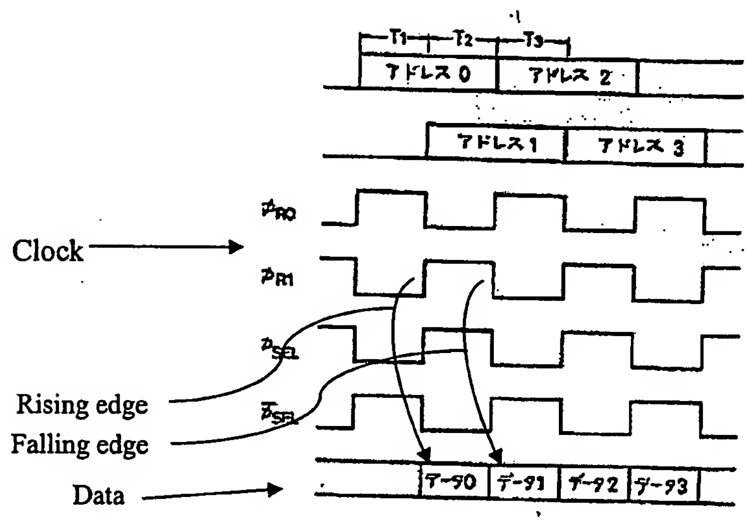
<u>The iAPX Manual in view of Yoshida</u>

43) Claims 3, 18, and 31 are rendered obvious by the iAPX Manual in view of Japanese Patent JP S56-047996 to Yoshida ("Yoshida"). A copy of Yoshida, along with an English translation, is provided at Exhibit I. Following the claim analysis below is a discussion of the motivation to combine these two references.

As discussed above, the iAPX Manual teaches all of the limitations to claims 1, 16, and 26, upon which claims 3, 18, and 31 depend, respectively. The iAPX Manual does not specifically discuss, however, a double data rate in which data is accessed on both the rising and falling edge transitions of the external clock.

Yoshida teaches a semiconductor memory device that is based on two external clock signals that are 180 degrees out of phase, as illustrated by clock signal θ_{R0} and θ_{R1} in the figure below. By having two clock signals exactly out of phase, Yoshida teaches a memory device that outputs data at a double data rate (a rate that is double that of a conventional device, which outputs data once each clock cycle). That is, Yoshida teaches that a first portion of data is output synchronously with respect to a rising edge transition of an external clock and a second portion of data is output synchronously with respect to a falling edge transition of an external clock.[36]

[36] Note that the specification of the '916 patent does not disclose outputting data on both the rising and falling edge of an <u>external</u> clock signal. At best, the disclosure indicates that two internal clocks (CLK and /CLK) could operate at half the bus data rate and, if each clock outputs data on one of its edges (as is done traditionally), the device could output data at the same rate as the bus clock. See Fig. 10 and col. 21, lns. 53-62.



One skilled in the art would be motivated to combine the iAPX Manual and Yoshida based on the teachings of Yoshida and due to the nature of the problem to be solved. Both the iAPX Manual and Yoshida are directed to semiconductor memory devices. The iAPX Manual recognizes the need for more memory bandwidth, and provides a solution of requesting additional memory buses. Pg. 1-2. Also, the iAPX Manual creates a pipeline, in which a memory bus can queue up to three memory requests at a time. Pg. 1-5. Yoshida also recognizes the need for increased bandwidth, and provides a different solution – memory accesses during rising and falling edges of a clocked input. "[A]n object of the present invention is to provide a semiconductor memory device that is capable of faster operation." Pg. 541, section 4. Yoshida therefore addresses a stated need of the iAPX Manual. Upon reviewing Yoshida and the disclosed faster memory operation, one skilled in the art at the time of the invention of the '916 patent would have been motivated to apply the teachings of Yoshida to the iAPX Manual to provide a bus access scheme in which data is sampled on rising and falling edges of a clock to expedite the handling of outstanding memory access requests. This modification would be made for both read and write accesses because both are supported similarly by the multiplexed bus of the iAPX Manual. A reasonable expectation of success exists because the iAPX Manual already anticipates that the component clock for the MCU can be changed. Pg. C-25. Also, the Yoshida double clock would work well at emptying the pipeline of memory requests on the iAPX's memory bus.

The iAPX Manual in view of Olson

44) Claim 9 is rendered obvious based on the iAPX Manual in view of U.S. Patent No. 4,933,910 to Olson ("Olson", Exhibit J). As discussed above, the iAPX Manual describes all of the limitations of claim 1, upon which claim 9 depends. To the extent Rambus asserts that one or more control signals can be an operation code, Olson teaches a method of including precharge information in an operation code, as required in claim 9.

Specifically, Olson describes accessing memory in either page mode (which does not precharge) or non-page mode (conventional). A memory controller selectively activates control signals MEMPAGE and MEMCYCLE to control precharging of the memory. Col. 2, lns. 40-44; col. 3, lns. 28-30, 52-60. Olson teaches that "the occurrence of an idle cycle will not transfer control" to a state where RAS and CAS are held inactive, but rather, will result in RAS and CAS remaining active. Col. 4, lns. 16-57. Thus, by keeping RAS active during idle cycles, RAS precharge is not necessary for a quick page access of the previously accessed page.

One skilled in the art would have been motivated to combine the iAPX Manual and Olson due to the nature of the problem to be solved. Both the iAPX Manual and Olson are directed to semiconductor memory devices with attached, local memory controllers (See Fig. 1 of Olson, memory array 12 and local memory controller 34). The iAPX Manual provides a pipelined memory bus capable of holding as many as three memory requests at a time. The MCU responds to the memory requests by providing blocks of data for each request. Each reply by the MCU therefore removes one request from the pipeline. Pg. 1-5. The iAPX Manual thus recognizes the problem of a full pipeline and waiting for an MCU to respond. Olson discloses a method of selectively sending precharge information with a memory read operation to thereby reduce the access time of memory accesses on page boundaries. This works especially well when a contiguous block of data is being requested, as in the iAPX Manual. In this regard, one skilled in the art would have been motivated to combine the teachings of the iAPX Manual and Olson to more efficiently access contiguous blocks of data. One skilled in the art would have been motivated to form such a combination to reduce the time a memory access request is queued, thereby increasing memory access request throughput. Furthermore, since the iAPX Manual is a packetized system of communication, additional room in the packet for precharge information can be readily accommodated, thereby providing a reasonable expectation of success.

The iAPX Manual in view of Grover

45) Claim 40 is rendered obvious by the iAPX Manual in view of U.S. Patent No. 5,361,277 to Grover ("Grover", Exhibit K). As discussed above, independent claim 26, upon which claim 40 depends, is anticipated by the iAPX Manual. Grover teaches clock circuitry to generate an internal clock signal for use by output drivers.

Grover discloses a method and apparatus for "synchronizing a plurality of spatially distributed application modules having synchronizing clocks requiring synchronization." Abstract. As shown in Fig. 6a of Grover, two external clock inputs, P1 and P2, are fed to binary counters of a clock circuit. Using a comparator, buffers, a voltage controlled oscillator, and appropriate divider circuits, a single "application clock" (*internal clock signal*) is derived from the pair of external clock signals. It is noted that the clock circuitry of Grover is extremely similar to the clock circuitry described in Fig. 12 of the '916 patent. To the extent Rambus asserts that the internal clock circuitry in Fig. 12 of the '916 patent is a DLL, then Grover in combination with the iAPX Manual disclose claim 40 of the '916 patent.

Motivation to combine the iAPX Manual and Grover comes from the teachings of Grover. Grover recognizes a problem in systems like the iAPX Manual, in which multiple modules are connected to a shared clock of a high speed memory bus. "[T]he basic problem is that of 'clock distribution' to a large number of state devices distributed over a distance where propagation delays are a significant fraction of the clock period[.]" Col. 1, lns. 34-38. Grover then provides the above-described clock circuit that produces an internal clock signal with a phase that is in synch with the internal clocks of other devices on the same bus. So following Grover's suggestion, one of ordinary skill in the art would be motivated to add Grover's clock circuit to the memory modules of the iAPX system. A reasonable expectation of success exists because Grover's clock circuit is self-contained, that is, it receives an out-of-phase clock signal and produces an in-phase internal clock signal without any further modifications to the memory module.

The iAPX Manual in view of Lofgren

46) Claim 40 is rendered obvious by the iAPX Manual in view of GB 2197553 to Lofgren et al. ("Lofgren", Exhibit L). As discussed above, independent claim 26, upon which claim 40 depends, is anticipated by the iAPX Manual. Lofgren teaches that a phase lock loop

with a variable delay (now commonly understood to be a DLL) can be used to control "high speed dynamic RAM devices, which comprise the main memory of virtually all personal computers." Abstract. In this regard, Lofgren discloses "[a] circuit for providing precise delays [that] includes a phase-locked loop ... and including a variable delay circuit 12." Abstract. The delay circuit provides "an output signal which is delayed by a precise amount with respect to an input signal." Pg. 1, lns. 8-10. Lofgren teaches that the variable delay circuit provides "a delay line with precise desired delays." Pg. 1, lns. 105-106.

Motivation to combine the iAPX Manual and Lofgren comes from the teachings of Lofgren. Lofgren recognizes the problem in systems like those in the iAPX Manual, in which a high speed dynamic memory device is controlled to operate with clocked delay. As described above, the iAPX Manual teaches read and write latency that is controlled based on a clocked signal. Lofgren then provides a solution to achieve precise delays. So following Lofgren's suggestion, one of ordinary skill in the art would be motivated to add Lofgren's DLL circuit to the memory modules of the iAPX system. A reasonable expectation of success exists because Lofgren's DLL circuit is self-contained, that is, it reduces the error between a clocked input signal and a clocked output signal without any further modifications to the memory module.

<u>The iAPX Manual in view of the iRAM reference</u>

47) In the alternative to the anticipation arguments provided above with respect to independent claims 1, 15, and 26, Requester submits that these claims are rendered obvious by the iAPX Manual in view of Intel Corporation, <u>Memory Components Handbook</u>, ("the iRAM reference," Exhibit N). Furthermore, claims 2, 4-8, 10-14, 16-17, 19-25, 28-30, 32-39, and 41 depend on these claims, and are further rendered obvious. Following the claim analysis below is a discussion of the motivation to combine these two references.

To the extent Rambus alleges that these claims require a single integrated circuit, one of skill would have known that the functionality of the controller and the memory (collectively referred to as the memory module in the iAPX Manual) could be combined on a single chip in accordance with the general trend toward integrating controller and memory functionality on a single integrated circuit. See MPEP § 2143.01. One example of a prior art reference that suggests the desirability to integrate control and memory functionality onto a single integrated circuit is the iRAM reference. "An integrated RAM or iRAM integrates a dynamic RAM and its

control and refresh circuitry on one substrate[.]"[37] It is important to note that the EPO Opposition Division came to a similar determination finding that the iRAM reference "appears to confirm the general tendency towards higher levels of integration also in the area of memory control" and that there was no evidence "to demonstrate convincingly that the skilled person would have resisted the general trend towards higher integration and would not have combined the [controller] and the DRAM described in D30 on a single chip." Exhibit AF at § 6.5.

It would at least be obvious to combine the controller and the memory of the iAPX Manual onto a single chip in light of the iRAM reference. Both the iAPX Manual and the iRAM reference describe memory systems that interact with a microprocessor. The iRAM teaches that integrating the entire dynamic RAM system on a chip has several advantages: "[t]his new implementation combines the cost, power and density advantages of a DRAM with the ease of use of a static RAM. Because all of the DRAM control logic is internal, the memory system can operate autonomously, controlling its own refresh and arbitration. This greatly simplifies microprocessor interfacing and minimizes additional TTL hardware support." Exhibit N at pg. 3-41.

<u>Budde in view of Rau</u>

48) In the alternative to the anticipation arguments provided above with respect to claims 1, 14, 15, 19, and 26-28, Requester submits that these claims are rendered obvious by Budde in view of <u>The Cydra 5 Departmental Supercomputer Design Philosophies, Decisions, and Tradeoffs</u> paper ("Rau"). Furthermore, claims 2, 4-8, 10-13, 16-17, 20-25, 29-30, 32-39, and 41 depend on these claims, and are further rendered obvious. Following the claim analysis below is a discussion of the motivation to combine these two references.

Regarding claims 1, 14, 15, 19, and 26-28, Budde describes receiving a memory access time value that indicates a number of clock cycles the memory waits to respond to a read request. Rau similarly teaches that this value can be provided by an attached numeric processor. Specifically, Rau teaches a memory system that includes a "memory latency register" (MLR) that receives a "value of the memory latency" from a numeric processor. Pgs. 31, 33. The

[37] Id. at pg. 1-2. See also, pg. 3-432 which discusses the general desire to integrate the "extensive control and interface requirements" for a DRAM onto a single, simple to use and high performance device.

memory system will buffer any output data being read from the memory system for the number of "numeric processor cycles" stored in the memory latency register. Pg. 33. "The MLR allows the compiler to treat memory accesses as having a deterministic latency but to use different values for the latency in different portions of the code so as to always deliver near-optimal performance." Pg. 33.

As for claims 28, 30, 32-39, and 41, as set forth in the anticipation arguments provided above, Budde describes the additional limitations in these claims.

One skilled in the art would be motivated to combine Budde and Rau based on the teachings of Rau and due to the nature of the problem to be solved. Both Budde and Rau are directed to computer and memory systems connected by a common bus, and modifying the interface there between. Budde recognizes the problem that memory latency needs to be modified for different reasons (including not limiting the system to the longest contemplated latency), and therefore provides an initialization procedure which provides a *value representative of a number of clock cycles to transpire before responding to the memory request.* Rau recognizes this same problem, but further recognizes that having the processor set the value for the memory latency provides "near-optimal performance." Pg. 33. Upon reviewing Rau and the identified benefits of having the processor set the memory latency value to the minimum value based on the particular type of code that is executing, one skilled in the art would have been motivated to combine the teachings of Budde and Rau to provide the memory latency from an external source.

In addition, Budde describes a stated desire to have a modular system of sufficient flexibility to meet specific needs. See col. 2, lns. 17-18. Furthermore, Budde teaches that "[e]ach MCU controls a single 256K byte to 4M byte dynamic memory array." Col. 3, ln. 68 through col. 4, ln. 1. However, in order to achieve this flexibility, "[e]ach MCU in the system logically attaches to one of the memory buses (MACD) and controls a single four-byte-wide array of memory." Col. 4, lns. 10-12. Budde teaches that a "time-ordered memory bus arbitration scheme ...guarantees access indivisibility." Col. 4, lns. 7-9. Rau discusses a similar system with a memory latency value provided from a hardware/hardwired solution: "This made us nervous about hardwiring the nominal memory latency value into the compiler and the hardware." Pg. 33. As a result, Rau proposed a modification to such systems by having the memory latency value being provided from an external processor. Thus, upon reading Rau, one

of ordinary skill in the art would be motivated to modify the teachings of Budde to similarly have the memory latency value provided by the processor.

A reasonable expectation of success exists because Budde already describes providing various types of control information over the external MACD bus during the same initialization cycle, and also describes providing a value for memory latency to the MCU.

<u>Budde in view of Yoshida</u>

49) Claims 3, 18, and 31 are rendered obvious by Budde in view of Japanese Patent JP S56-047996 to Yoshida ("Yoshida"). Following the claim analysis below is a discussion of the motivation to combine these two references.

As discussed above, Budde teaches all of the limitations to claims 1, 16, and 26, upon which claims 3, 18, and 31 depend, respectively. Budde does not specifically discuss, however, a double data rate in which data is accessed on both the rising and falling edge transitions of the external clock.

As described above in paragraph 43), Yoshida teaches a semiconductor memory device that is based on two external clock signals that are 180 degrees out of phase. By having two clock signals exactly out of phase, Yoshida teaches a memory device that outputs data at a double data rate. That is, as previously shown, Yoshida teaches that *a first portion of data is output synchronously with respect to a rising edge transition of an external clock* and teaches that *a second portion of data is output synchronously with respect to a falling edge transition of the same external clock.*

One skilled in the art would be motivated to combine Budde and Yoshida based on the teachings of Yoshida and due to the nature of the problem to be solved. Both Budde and Yoshida are directed to semiconductor memory devices. Budde recognizes the need for a time-ordered allocation of memory access requests in a pipeline. One skilled in the art, upon review of Budde, would recognize the need to increase the speed by which memory access requests are handled to reduce the occurrences of memory access requests being withheld from the pipeline because the number of outstanding memory access requests is at the maximum allowed. Yoshida recognizes the need for increased bandwidth, and provides a solution – memory accesses during rising and falling edges of a clocked input. "[A]n object of the present invention is to provide a semiconductor memory device that is capable of faster operation." Pg. 541,

section 4. Yoshida therefore addresses a need of Budde. Upon reviewing Yoshida and the need for faster memory operation, one skilled in the art at the time of the invention of the '916 patent would have been motivated to combine the teachings of Budde and Yoshida to provide a bus access scheme in which data is sampled on rising and falling edges of a clock to expedite the handling of outstanding memory access requests. This combination would reasonably be made for both read and write accesses because both are supported similarly by the bus of Budde. A reasonable expectation of success exists because Budde already provides a FIFO for sending and receiving data, and the FIFO can be clocked at a double data rate.

Budde in view of Olson

50) Claim 9 is rendered obvious based on Budde in view of U.S. Patent No. 4,933,910 ("Olson"). As discussed above, Budde describes all of the limitations of claim 1, upon which claim 9 depends. Olson teaches a method of including precharge information in an operation code, as required in claim 9.

Specifically, Olson describes accessing memory in either page mode (which does not precharge) or non-page mode (conventional). A memory controller selectively activates control signals MEMPAGE and MEMCYCLE to control precharging of the memory. Col. 2, lns. 40-44; col. 3, lns. 28-30, 52-60. To the extent Rambus asserts that one or more control signals can be an operation code, Olson teaches that "the occurrence of an idle cycle will not transfer control" to a state where RAS and CAS are held inactive, but rather, will result in RAS and CAS remaining active. Col. 4, lns. 16-57. Thus, by keeping RAS active during idle cycles, RAS precharge is not necessary for a quick page access of the previously accessed page.

One skilled in the art would have been motivated to combine Budde and Olson due to the nature of the problem to be solved. Both Budde and Olson are directed to semiconductor memory devices with attached, local memory controllers (See Fig. 1 of Olson, memory array 12 and local memory controller 34). Budde provides a pipelined memory bus. The MCU responds to the memory requests by providing blocks of data for each request. Each reply by the MCU therefore removes one request from the pipeline. Budde thus recognizes the problem of a full pipeline and waiting for an MCU to respond. Olson discloses a method of sending precharge information with a memory read operation that reduces the access time of memory accesses on page boundaries. This works especially well when a contiguous block of data is being requested,

as in Budde. In this regard, one skilled in the art would have been motivated to combine the teachings of Budde and Olson to more efficiently access contiguous blocks of data. One skilled in the art would have been motivated to form such a combination to reduce the time a memory access request is queued, thereby increasing memory access request throughput. Furthermore, since Budde discloses a packetized system of communication, additional room in the packet for precharge information can be readily accommodated, thereby providing a reasonable expectation of success.

Budde in view of Grover

51) Claim 40 is rendered obvious by U.S. Patent 4,480,307 in view of U.S. Patent No. 5,361,277 ("Grover"). As discussed above, independent claim 26, upon which claim 40 depends, is anticipated by Budde. Grover teaches clock circuitry to generate an internal clock signal for use by output drivers.

Grover discloses a method and apparatus for "synchronizing a plurality of spatially distributed application modules having synchronizing clocks requiring synchronization." Abstract. As shown in Fig. 6a of Grover, two external clock inputs, P1 and P2, are fed to binary counters of a clock circuit. Using a comparator, buffers, a voltage controlled oscillator, and appropriate divider circuits, a single "application clock" (*internal clock signal*) is derived from the pair of external clock signals. It is noted that the clock circuitry of Grover is almost identical to the clock circuitry described in Fig. 12 of the '916 patent. To the extent Rambus asserts that the internal clock circuitry in Fig. 12 of the '916 patent is a DLL, then Grover in combination with the iAPX Manual disclose claim 40 of the '916 patent.

Motivation to combine Budde and Grover comes from Grover itself. Grover recognizes a problem in systems like that of Budde, in which multiple modules are connected to a shared clock of a high speed memory bus. "[T]he basic problem is that of 'clock distribution' to a large number of state devices distributed over a distance where propagation delays are a significant fraction of the clock period[.]" Col. 1, lns. 34-38. Grover then provides the above-described clock circuit that produces an internal clock signal with a phase that is in synch with the internal clocks of other devices on the same bus. So following Grover's suggestion, one of ordinary skill in the art would be motivated to add Grover's clock circuit to the memory modules of Budde. A reasonable expectation of success exists because Grover's clock circuit is self-contained, that is,

it receives an out-of-phase clock signal and produces an in-phase internal clock signal without any further modifications to the memory module.

<u>Budde in view of Lofgren</u>

52) Claim 40 is rendered obvious by Budde in view of GB 2197553 to Lofgren et al. ("Lofgren"). As discussed above, independent claim 26, upon which claim 40 depends, is anticipated by Budde. Lofgren teaches that a phase lock loop with a variable delay (now commonly understood to be a DLL) can be used to control "high speed dynamic RAM devices, which comprise the main memory of virtually all personal computers." Abstract. In this regard, Lofgren discloses "[a] circuit for providing precise delays [that] includes a phase-locked loop ... and including a variable delay circuit 12." Abstract. The delay circuit provides "an output signal which is delayed by a precise amount with respect to an input signal." Pg. 1, lns. 8-10. Lofgren teaches that the variable delay circuit provides "a delay line with precise desired delays." Pg. 1, lns. 105-106.

Motivation to combine Budde and Lofgren comes from the teachings of Lofgren. Lofgren recognizes the problem in systems like those of Budde, in which a high speed dynamic memory device is controlled to operate with clocked delay. As described above, Budde teaches read and write latency that is controlled based on a clocked signal. Lofgren then provides a solution to achieve precise delays. So following Lofgren's suggestion, one of ordinary skill in the art would be motivated to add Lofgren's DLL circuit to the memory modules of Budde. A reasonable expectation of success exists because Lofgren's DLL circuit is self-contained, that is, it reduces the error between a clocked input signal and a clocked output signal without any further modifications to the memory module.

<u>Budde in view of the iRAM reference</u>

53) In the alternative to the anticipation arguments provided above with respect to independent claims 1, 15, and 26, Requester submits that these claims are rendered obvious by Budde in view of Intel Corporation, <u>Memory Components Handbook</u> ("the iRAM reference," Exhibit N). Furthermore, claims 2, 4-8, 10-14, 16-17, 19-25, 28-30, 32-39, and 41 depend on these claims, and are further rendered obvious. Following the claim analysis below is a discussion of the motivation to combine these two references.

To the extent Rambus alleges that these claims require a single integrated circuit, one of skill would have known that the functionality of the controller and the memory (collectively referred to as the memory module in Budde) could be combined on a single chip in accordance with the general trend toward integrating controller and memory functionality on a single integrated circuit. See MPEP § 2143.01. One example of a prior art reference that suggests the desirability to integrate control and memory functionality onto a single integrated circuit is the iRAM reference. "An integrated RAM or iRAM integrates a dynamic RAM and its control and refresh circuitry on one substrate[.]"[38] It is important to note that the EPO Opposition Division came to a similar determination finding that the iRAM reference "appears to confirm the general tendency towards higher levels of integration also in the area of memory control" and that there was no evidence "to demonstrate convincingly that the skilled person would have resisted the general trend towards higher integration and would not have combined the [controller] and the DRAM described in D30 on a single chip." Exhibit AF at § 6.5.

It would at least be obvious to combine the controller and the memory of Budde onto a single chip in light of the iRAM reference. Both Budde and the iRAM reference describe memory systems that interact with a microprocessor. The iRAM teaches that integrating the entire dynamic RAM system on a chip has several advantages: "[t]his new implementation combines the cost, power and density advantages of a DRAM with the ease of use of a static RAM. Because all of the DRAM control logic is internal, the memory system can operate autonomously, controlling its own refresh and arbitration. This greatly simplifies microprocessor interfacing and minimizes additional TTL hardware support." Exhibit N at pg. 3-41.

III. Statement Pointing Out Substantial New Question Of Patentability

The prior art documents referred to above are not of record in the file of the '916 patent. Since claims 1-41 in the '916 patent are not patentable over these prior art documents, a substantial new question of patentability is raised.

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38 Id. at pg. 1-2. See also, pg. 3-432 which discusses the general desire to integrate the "extensive control and interface requirements" for a DRAM onto a single, simple to use and high performance device.

IV. List of Exhibits

Exhibit A	Farmwald et al., U.S. Patent No. 6,426,916 issued July 30, 2002 ("the '916 patent")
Exhibit B	Park et al., U.S. Patent No. 5,590,086 issued December 31, 1996 ("Park")
Exhibit C	Joint Electron Device Engineering Council (JEDEC) Standard No. 21-C, Revision 9 published in 1999 ("JEDEC Standard")
Exhibit D, Tab 1	Hyundai, HY5DV651622, Rev. 0.9, published January 2000 ("Hynix -1")[39]
Exhibit D, Tab 2	Hyundai, SDRAM Timing Diagram, Rev. 1.2, published December 1999 ("Hynix -2")
Exhibit D, Tab 3	Hyundai, DDR SDRAM DEVICE OPERATION, Rev. 0.2, published December 1998 ("Hynix -3")
Exhibit E, Tab 1	Intel Corporation, iAPX 432 Interconnect Architecture Reference Manual, published in 1982 ("the iAPX Manual")
Exhibit E, Tab 2	Intel Corporation, Electrical Specifications for iAPX 43204 Bus-Interface Unit (BIU) and iAPX 43205 memory control unit (MCU), published March 1983 ("the iAPX Specification")
Exhibit F	Budde et al., U.S. Patent No. 4,480,307 issued October 30, 1984 ("Budde")
Exhibit G	Jackson, U.S. Patent No. 4,315,308 issued February 9, 1982 ("the '308 patent")
Exhibit H	Rau et al., The Cydra 5 Departmental Supercomputer Design Philosophies, Decisions, and Tradeoffs, published in January 1989 ("Rau")
Exhibit I	Yoshida, Japanese Patent JP S56-047996 published April 30, 1981, English translation provided ("Yoshida")
Exhibit J	Olson et al., U.S. Patent No. 4,933,910 issued June 12, 1990 ("Olson")
Exhibit K	Grover, U.S. Patent No. 5,361,277 filed March 30, 1989, issued November 1, 1994 ("Grover")
Exhibit L	Lofgren et al., UK published patent app. No. GB2197553, published May 18, 1988 ("Lofgren")
Exhibit M	Johnson et al., A Variable Delay Line PLL for CPU – Coprocessor Synchronization, IEEE Journal of Solid-State Circuits, vol. 23, no. 5, published

[39] Hyundai Electronics became Hynix.

October 1988 ("Johnson")

Exhibit N	Intel Corporation, Memory Components Handbook, Chapter 1 and Chapter 3, Application Note AP-132, published in 1982 and 1985 ("the iRAM reference")
Exhibit O	Claim chart for claims 1-5, 10, 12-16, 18-20, 23, 25-32, 35, 37, and 39-41 based on Park, with additional reference to the JEDEC Standard
Exhibit P	Claim chart for claims 1-5, 9-10, 12-16, 18-20, 23, 25-27, 30-32, 35, 37, and 40-41 based on the JEDEC Standard
Exhibit Q	Claim chart for claims 1-41 of the '916 patent based on the iAPX Manual, with additional reference to Rau, Yoshida, Olson, Johnson, Lofgren, and Grover
Exhibit R	Claim chart for claims 1-41 of the '916 patent based on Budde, with additional reference to Rau, Yoshida, Olson, Johnson, Lofgren, and Grover
Exhibit S	Patent Family Tree Chart
Exhibit T	File History of the '916 patent
Exhibit U	File History of U.S. Patent No. 6,452,863 ("the '863 parent patent") (Tab 1 identifies the original disclosure of the '863 parent patent, and Tab 2 identifies the remaining portions of the file history)
Exhibit V	*Rambus Inc. v. Samsung Electronics Ltd., et al.* No. C 05 02298 RMW (N.D. Cal. 2006), Preliminary Infringement Contentions
Exhibit W	*Samsung Electronics Co., Ltd., v. Rambus Inc.* No. 3:05cv406 (E.D. Va. 2006), Memorandum Opinion filed July 18, 2006
Exhibit X	*Hynix Semiconductor, Inc. et al. v. Rambus Inc.*, No. CV 00-20905 RMW (N.D. Cal. 2005), Joint Claim Construction and Prehearing Statement Pursuant to Patent Local Rule 4-3
Exhibit Y	*Hynix Semiconductor, Inc. et al. v. Rambus Inc.*, No. CV 00-20905 RMW (N.D. Cal. 2005), Claim Construction Order filed Nov. 15, 2004 .
Exhibit Z	Selected Excerpts from the Trial Transcript from *Hynix Semiconductor, Inc. et al. v. Rambus Inc.*, No. CV 00-20905 RMW (N.D. Cal. 2005).
Exhibit AA	*Rambus Inc. v. Infineon Technologies et al.*, No. 3:00cv524 (E.D. Vir. 2001), Memorandum Opinion
Exhibit AB	*Rambus Inc. v. Infineon Technologies AG,* 318 F.3d 1081 (Fed. Cir. 2003)
Exhibit AC	Waters, Hynix Told To Pay Damages To Rambus, Financial Times, April 24 2006

Exhibit AD	Poletti, Rambus wins victory from Supreme Court - Win Could Lead To Success For Rambus' Other Lawsuits Seeking Royalties, San Jose Mercury News, Oct. 07, 2003
Exhibit AE	Kanellos, Future of memory market hangs on Rambus trials - It's the trial of the century, at least as far as the memory industry is concerned, CNET News.com, Feb. 12, 2001, http://news.com.com/Future+of+memory+market+hangs+on +Rambus+trials/2100-1001_3-252404.html
Exhibit AF	Appeal Board Decision dated Feb. 12, 2004, Summary of Facts and Submissions for the oppositions filed against European Patent No. 0 525 068
Exhibit AG	Summary of Facts and Submissions for the oppositions filed against European Patent No. 1 004 956
Exhibit AH, Tab 1	In the Matter of Rambus, Inc., FTC Docket No. 9302, Opinion of the Commission
Exhibit AH, Tab 2	In the Matter of Rambus, Inc., FTC Docket No. 9302, Concurring Opinion of Commissioner Jon Leibowitz
Exhibit AH, Tab 3	In the Matter of Rambus, Inc., FTC Opinion Docket No. 9302, Order Reversing and Vacating Initial Decision ...
Exhibit AI, Tab 1	Rambus' Final infringement Contentions in the Hynix Litigation
Exhibit AI, Tab 2	Exhibit A (accused products) to Rambus' Final infringement Contentions
Exhibit AI, Tab 3	Exhibit P ('916 infringement chart) to Rambus' Final infringement Contentions
Exhibit AI, Tab 4	Exhibit R (Exemplary data sheet) to Rambus' Final infringement Contentions
Exhibit AJ	CD-ROM including present Request for *Inter Partes* Reexamination and Exhibits

V. Conclusion

For at least the reasons set forth above, it is clear that a new question of patentability is raised in connection with claims 1-41 by this Request for *Inter Partes* Reexamination since claims 1-41 are anticipated and/or rendered obvious in view of the above-listed prior art references. Therefore, it is requested that this request for reexamination be granted and claims 1-41 all be finally rejected.

As identified in the attached Certificate of Service and in accordance with 37 CFR §§133(c) and 1915(b)(6), a copy of the present request, in its entirety, is being served to the address of the attorney or agent of record.

Please direct all correspondence in this matter to the undersigned.

Respectfully submitted,

David L. McCombs
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Dated: August 8, 2006

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CERTIFICATE OF SERVICE

The undersigned certifies that copies of the following:

(1) Request for *Inter Partes* Reexamination Transmittal Form; and

(2) Request for *Inter Partes* Reexamination including Exhibits A through AJ

were served on

Jose Moniz
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the attorney of record for the assignee of USP 6,426,916 in accordance with 37 CFR § 1915(b)(6), on the 8th day of August, 2006

David L. McCombs